ATCA-7367

Installation and Use

P/N: 6806800K72N

September 2015

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About this Manual

Overview of Contents

This Reference Guide is intended for users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), AdvancedTCA®, and telecommunications.

The manual contains the following chapters and appendices:

- *About this Manual* on page 15 lists all conventions and abbreviations used in this manual and outlines the revision history.
- *Safety Notes* on page 25 lists safety notes applicable to the blade.
- *Sicherheitshinweise* on page 29 provides the German translation of the safety notes section.
- *Introduction* on page 35 describes the main features of the blade.
- *Hardware Preparation and Installation* on page 43 outlines the installation requirements, hardware accessories, switch settings, installation and removal procedures.
- *Controls, Indicators, and Connectors* on page 63 describes external interfaces of the blade. This includes connectors and LEDs.
- *BIOS* on page 77 describes the features and setup of BIOS.
- *Functional Description* on page 121 describes the functional blocks of the blade in detail. This includes a block diagram, description of the main components used and so on.
- *Maps and Registers* on page 135 provides information on the blade's maps and registers.
- *Serial Over LAN* on page 139 provides information on how to establish a serial-over LAN session on your blade.
- *Supported IPMI Commands* on page 145 lists all supported IPMI commands.
- *FRU Information and Sensor Data Records* on page 189 provides information on the blade's FRU information and sensor data.
- *Firmware Upgrade* on page 207 provides information on Firmware upgrade.
- *Replacing the Battery* on page 213 provides the procedures in changing the battery.
- *Related Documentation* on page 217 provides links to further blade-related documentation.

Abbreviations

This document uses the following abbreviations:

Abbreviation	Definition
AMC	Advanced Mezzanine Card
AMC.x	A generic reference to all AMC specifications (AMC.0, AMC.1, AMC.2, AMC.3)
AMC Bay	A single AMC site on an AMC carrier
ATCA	Advanced Telecom Compute Architecture
AVR	Atmel's 8-bit RISC micro-controller family
ATCA	Artesyn's AdvancedTCA Multi-service platform
BBS	Basic Blade Services
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BOM	Bill of Material
CFM	Cubic Feet per Minute
CG	Carrier-grade
CK409B	Clock generator standard for Intel chipset platforms
CPLD	Complex Programmable Logic Device
CPM	Critical Parameter Management
CPU	Central Processing Unit
DDR	Dual Data Rate (type of SDRAM)
DDR3	Double Data Rate 3 synchronous dynamic random access memory (SDRAM) is the name of the new DDR memory standard that is being developed as the successor to DDR2 SDRAM.
DFM	Design for Manufacturability
DFT	Design for Test
DMA	Direct Memory Access

Abbreviation	Definition
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electro-magnetic Compatibility
EMI	Electro-magnetic Interference
ESD	Electro-static Discharge
FMECA	Failure Mode, Effects and Criticality Analysis
FRU	Field Replaceable Unit
FSB	Front-side Bus
FWH	Firmware Hub
GA	General Availability
Gb	Gigabit(s)
GB	Gigabyte(s)
Gbps	Gigabits per second
GHz	Gigahertz
GigE	Gigabit Ethernet
GPIO	General Purpose Input/Output
I2C	Inter Integrated-Circuit Bus (2-wire serial bus and protocol)
I/O	Input/Output
IA-32	32-bit Intel processor architecture
ICH	I/O Control Hub (also called "South Bridge")
ICT	In-circuit Test
IMC	Integrated Memory Controller
IPMB	Intelligent Platform Management Bus
IPMB-L	The IPMB connecting the carrier IPMC to the AMC module
Intel® QuickPath Interconnect (Intel® QPI)	A cache-coherent, link-based Interconnect specification for Intel processors, chipsets, and I/O bridge components.
MMC	Intelligent Platform Management Controller

Abbreviation	Definition
IPMI	Intelligent Platform Management Interface
ITP	In-Target Probe
ITP700	An ITP scheme defined by Intel
JTAG	Joint Test Action Group (test interface for digital logic circuits)
L2	Level 2 (as in "L2 Cache")
LAN	Local Area Network
LED	Light-emitting Diode
LFM	Linear Feet per Minute
LPC	Low Pin Count
LVDS	Low Voltage Differential Signaling
MAC	Medium Access Controller
Mb(ps)	Megabits (per second)
MB(ps)	Megabytes (per second)
MCH	Memory Controller Hub (also called "North Bridge")
MHz	Megahertz
MMC	Module Management Controller
Module	This term is used to refer to the Module card in this document
MP	Management Power
MTBF	Mean Time Between Failures
MTTR	Mean Time To Repair
N/A	Not Applicable
NEBS	Network Equipment Building System
NMI	Non-maskable Interrupt
NT	Non-transparent
NVRAM	Non-volatile Random Access Memory
OEM	Original Equipment Manufacturer
OOS	Out-of-service
OS	Operating System

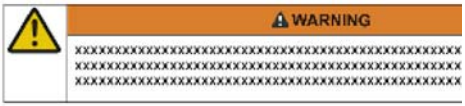
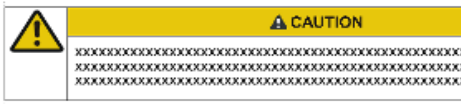
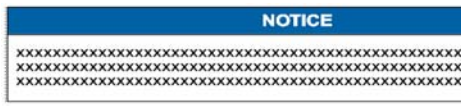
Abbreviation	Definition
PCB	Printed Circuit Board
PCI-E	PCI-Express
PHY	Physical layer device (for ethernet)
PICMG	PCI Industrial Computer Manufacturers Group
PLL	Phase Locked Loop
POST	Power-on Self Test
PP	Payload Power
PRD	Product Requirements Document
RC	Root Complex
RoHS	Restriction of Hazardous Substances
RS232	Recommended Standard 232C - interface standard for serial communication
RTC	Real-Time Clock
Rx	Receive line (of a duplex serial communication interface)
SATA	Serial AT Attachment (high-speed serial interface standard for storage devices)
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SELV	Safety Extra Low Voltage
SerDes	Serializer-Deserializer
SIMD	Single Instruction Multiple Data
SMBus	System Management Bus
SMI	System Management Interrupt
SODIMM	Small Outline Dual-in-line Memory Module
SPD	Serial Presence Detect
TBD	To be decided
TCP	Transmission Control Protocol
TDP	Thermal Design Power
Tx	Transmit line (of a duplex serial communication interface)

Abbreviation	Definition
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
VID	Voltage Identification (for Intel CPUs)
Westmere	Intel Codename for next gen.(after Core2Duo) Intel CPU microarchitecture
Tylersburg	Intel Codename for Intel IOH36D device
Zoar	Intel Codename for Intel 82576 Ethernet device

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
0x00000000	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
0b0000	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands in body text
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12

Notation	Description
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury
	Indicates a property damage message
	No danger encountered. Pay attention to important information

Summary of Changes

Part Number	Publication Date	Description
6806800K72N	September 2015	Updated ATCA-7367 IPMC information in Table 9-9 on page 199. Updated the sections *Standard Compliances* on page 37, *Installation* on page 26, and *Installation* on page 30.
6806800K72M	June 2014	Re-branded to Artesyn.
6806800K72L	February 2014	Updated Table "Sensor Data Records" on page 199 and Table "Face Plate LEDs" on page 67. Updated Table "Get Handle Switch Command Description" on page 177 and Table "Set Handle Switch Command Description" on page 178. Added a new section *IPMI Boot Parameter* on page 85, updated the sections *Advanced Menu* on page 92, *IPMI Menu* on page 103, updated the *System Boot Options Parameter #100 - Supported Parameters* on page 156. Added a new section *Event Logs Menu* under *BIOS Setup Utility* section.
6806800K72K	September 2012	Updated Table 4-22 and Chapter 7, *Using Standard IPMI Commands, on page 140*.
6806800K72J	April 2012	Updated Table "Switch SW3 Settings" on page 49.
6806800K72H	March 2012	Added a Note in *Standard Compliances* on page 37. Added Notice in *Installation* on page 26 and *Installation* on page 30. Updated *EMC* on page 25 and *EMV* on page 30.
6806800K72G	November 2011	Updated *Introduction* on page 77 and *BIOS Setup Utility* on page 89.
6806800K72F	September 2011	Updated Table "Sensor Data Records" on page 199.

Part Number	Publication Date	Description
6806800K72E	August 2011	Added *BIOS Setup Utility* on page 89. Updated Table "CPU Configuration" on page 93. Updated Table "Chipset - South Bridge" on page 97. Added Table "PCIE Root Ports Configuration" on page 98. Updated Figure "Boot Menu" on page 108.
6806800K72D	March 2011	Added Table "Sensor Data Records" on page 199 and Chapter 10, *Firmware Upgrade, on page 207*.
6806800K72C	January 2011	Updated *Zone 3* on page 73.
6806800K72B	June 2010	GA version
6806800K72A	April 2010	EA version

Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Artesyn Embedded Technologies intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Artesyn representative.

The product has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Artesyn or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product.

The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only factory authorized service personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local Artesyn representative for service and repair to make sure that all safety features are maintained.

EMC

The blade has been tested in a standard Artesyn system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules, EN 55022 Class A respectively. These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial environment.

This is a Class A product based on the standard of the Voluntary Control Council for Interference by Information Technology Interference (VCCI). If this equipment is used in a domestic environment, radio disturbance may arise. When such trouble occurs, the user may be required to take corrective actions.

To ensure EMC protection use only shielded cables when connecting peripherals to assure that appropriate radio frequency emissions compliance is maintained. Installed blades must have the face plates installed and all vacant slots in the shelf must be covered.

The blade generates and uses radio frequency energy and, if not installed properly and used in accordance with this guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Installation

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Data Loss
Removing the blade with the blue LED still blinking causes data loss.
Wait until the blue LED is permanently illuminated, before removing the blade.

Damage of Blade and Additional Devices and Modules
Incorrect installation of additional devices or modules may damage the blade or the additional devices or modules.
Before installing or removing an additional device or module, read the respective documentation

System Damage
WARNING: The intra-building port (s) of the equipment or subassembly is suitable for connection to intra-building or unexposed wiring or cabling only. The intra-building port (s) of the equipment or subassembly MUST NOT be metallically connected to interfaces that connect to the outside plant (OSP) or its wiring. These interfaces are designed for use as intra-building interfaces only (Type 2 or Type 4 ports as described in GR-1089) and require isolation from the exposed OSP cabling. The addition of primary protectors is not sufficient protection in order to connect these interfaces metallically to OSP wiring.
The intra-building port (s) of the equipment or subassembly must use shielded intra-building cabling/wiring that is grounded at both ends.

Operation

Blade Damage
Blade surface
High humidity and condensation on the blade surface causes short circuits.
Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power.

Blade Overheating and Blade Damage
Operating the blade without forced air cooling may lead to blade overheating and thus blade damage.
When operating the blade, make sure that forced air cooling is available in the shelf.

When operating the blade in areas of electromagnetic radiation ensure that the blade is bolted on the system and the system is shielded by enclosure.

Injuries or Short Circuits
Blade or power supply
In case the ORing diodes of the blade fail, the blade may trigger a short circuit between input line A and input line B so that line A remains powered even if it is disconnected from the power supply circuit (and vice versa).
To avoid damage or injuries, always check that there is no more voltage on the line that has been disconnected before continuing your work.

Switch Settings

Blade Malfunction
Switches marked as 'reserved' might carry production-related functions and can cause the blade to malfunction if their setting is changed.
Therefore, do not change settings of switches marked as 'reserved'. The setting of switches which are not marked as 'reserved' has to be checked and changed before blade installation.

Blade Damage
Setting/resetting the switches during operation can cause blade damage.
Therefore, check and change switch settings before you install the blade.

Battery

Blade Damage
Wrong battery installation may result in hazardous explosion and blade damage.
Therefore, always use the same type of Lithium battery as is installed and make sure the battery is installed as described in this manual.

Environment

Always dispose of used blades, system components and RTMs according to your country's legislation and manufacturer's instructions.

Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Produktes innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am Produkt zur Folge haben.

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EMV

Das Blade wurde in einem Artesyn Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Blades in Gewerbe- sowie Industriegebieten gewährleisten.

Das Blade arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.

Benutzen Sie zum Anschließen von Peripheriegeräten ausschließlich abgeschirmte Kabel. So stellen Sie sicher, dass ausreichend Schutz vor Störstrahlung vorhanden ist. Die Blades müssen mit der Frontblende installiert und alle freien Steckplätze müssen mit Blindblenden abgedeckt sein.

Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

Installation

Beschädigung von Schaltkreisen
Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau von Blades kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.
Bevor Sie Blades oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD-geschützten Bereich arbeiten.

Datenverlust
Wenn Sie das Blade aus dem Shelf herausziehen, und die blaue LED blinkt noch, gehen Daten verloren.
Warten Sie bis die blaue LED durchgehend leuchtet, bevor Sie das Blade herausziehen.

Beschädigung des Blades und von Zusatzmodulen
Fehlerhafte Installation von Zusatzmodulen, kann zur Beschädigung des Blades und der Zusatzmodule führen.
Lesen Sie daher vor der Installation von Zusatzmodulen die zugehörige Dokumentation.

Beschädigung des Systems
Warnung: Die intra-Gebäude Port (s) des Geräts oder Baugruppe ist für den Anschluss an den inner Gebäude oder unbelichteten Verdrahtung oder Verkabelung nur. Die intra-Gebäude Port (s) des Geräts oder Baugruppe muss nicht metallisch mit Schnittstellen, die an der Außenanlage (OSP) oder dessen Verkabelung anschließen angeschlossen werden. Diese Schnittstellen sind für die Verwendung als intra Gebäude Schnittstellen nur entworfen, (Typ 2 oder Typ 4 Ports wie in GR-1089 beschrieben) und erfordern Isolierung von der freiliegenden OSP-Verkabelung. Die Zugabe von primären Schutz nicht ausreichenden Schutz, um diese Schnittstellen metallisch mit OSP Verdrahtung verbinden.
Die intra-Gebäude Port (s) des Gerätes oder einer Unterbaugruppe müssen abgeschirmte innerGebäudeVerkabelung / Verdrahtung, die an beiden Enden geerdet ist zu verwenden.

Betrieb

Beschädigung des Blades
Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Blades können zu Kurzschlüssen führen.
Betreiben Sie das Blade nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Blade kein Kondensat befindet.

Überhitzung und Beschädigung des Blades
Betreiben Sie das Blade ohne Zwangsbelüftung, kann das Blade überhitzt und schließlich beschädigt werden.
Bevor Sie das Blade betreiben, müssen Sie sicher stellen, dass das Shelf über eine Zwangskühlung verfügt.

Wenn Sie das Blade in Gebieten mit starker elektromagnetischer Strahlung betreiben, stellen Sie sicher, dass das Blade mit dem System verschraubt ist und das System durch ein Gehäuse abgeschirmt wird.

Verletzungen oder Kurzschlüsse
Blade oder Stromversorgung
Falls die ORing Dioden des Blades durchbrennen, kann das Blade einen Kurzschluss zwischen den Eingangsleitungen A und B verursachen. In diesem Fall ist Leitung A immer noch unter Spannung, auch wenn sie vom Versorgungskreislauf getrennt ist (und umgekehrt).
Prüfen Sie deshalb immer, ob die Leitung spannungsfrei ist, bevor Sie Ihre Arbeit fortsetzen, um Schäden oder Verletzungen zu vermeiden.

Schaltereinstellungen

Fehlfunktion des Blades
Schalter, die mit 'Reserved' gekennzeichnet sind, können mit produktionsrelevanten Funktionen belegt sein. Das Ändern dieser Schalter kann im normalen Betrieb Störungen auslösen.
Verstellen Sie nur solche Schalter, die nicht mit 'Reserved' gekennzeichnet sind. Prüfen und ändern Sie die Einstellungen der nicht mit 'Reserved' gekennzeichneten Schalter, bevor Sie das Blade installieren.

Beschädigung der Blade
Das Verstellen von Schaltern während des laufenden Betriebes kann zur Beschädigung des Blades führen.
Prüfen und ändern Sie die Schaltereinstellungen, bevor Sie das Blade installieren.

Batterie

Beschädigung des Blades
Ein unsachgemäßer Einbau der Batterie kann gefährliche Explosionen und Beschädigungen des Blades zur Folge haben.
Verwenden Sie deshalb nur den Batterietyp, der auch bereits eingesetzt wurde und befolgen Sie die Installationsanleitung.

Umweltschutz

Entsorgen Sie alte Batterien und/oder Blades/Systemkomponenten/RTMs stets gemäß der in Ihrem Land gültigen Gesetzgebung und den Empfehlungen des Herstellers.

1.1 Features

ATCA-7367 is a high performance single processor AdvancedTCA Server blade and AdvancedTCA NODE board, designed according to PICMG 3.0 Revision 3.0 Advanced TCA Base Specification. ATCA-7367 is a single board computer that offers a powerful processing complex through a single six-core Intel Westmere-EP processor, and support for up to 48GB DDR3 memory. Furthermore ATCA-7367 provides local storage (Onboard SATA disk/SATA Cube, onboard flash disk, or through the RTM), standard I/O and redundant Gigabit Ethernet connections to the back plane's Base Interfaces (PICMG3.0) and Fabric Interfaces (PICMG 3.1 Option1,9). Another important feature is that ATCA-7367 provides AMC support and is compatible with different AMC boards to meet application-specific requirements. The ATCA-7367 provides system management capabilities and is hot swap compatible based on the ATCA specification.

The following lists the main feature of ATCA-7367:

- Form factor: Single slot ATCA (280mm x 322mm)
- Processor: Intel Westmere-EP Six-Core processor (Intel XEON 5600 series), Drop-in compatible with Intel Nehalem-EP processor (Intel XEON 5500 Series)
- North Bridge: Xeon 5520 (Tylersburg IOH36 D)
  - Provide two QPI interfaces for connecting to up to two Intel Xeon processors
  - Providing 36 PCI-e Gen2 lanes, Intel Virtualization Technology, ESI interface and Management Engine
  - FC-BGA 37.5mm x 37.5 mm, 1295 balls
- South Bridge: ICH10R, ESI connection to Xeon 5520 (Tylersburg IOH36 D)
  - Provides extensive I/O support and Boot path to redundant SPI Boot flashes
  - I/O interfaces include SATA, USB2.0, LAN, LPC interface, RTC with WDT
- Base interface : Dual 10/100/1000Base-T Ethernet
- Fabric Interface: Dual 1G/10Gbps Ethernet interfaces, support PICMG3.1 option 1 and 9
- Update Channel: One 10/100/1000Base-T, and SAS ports
- RTM Interface
  - Five PCI-e x4
  - 8-Port AMC I/O

  - 2x SAS Ports (SAS controller is on RTM)
  - 1x SATA port
  - 3x Telecom Clock
  - 1x UART and 1x USB interfaces
  - IPMI Management bus
- One AMC slot
  - GE on ports 0, 1, 8, 9, 10, 11
  - PCIe x4 on ports 4-7
  - SAS on port 2, SATA on port3
  - Port 13-20 to Zone 3
  - TCLK and FCLK support
- Front Panel
  - One 10/100/1000BASE-T Ethernet
  - Two USB2.0 Ports
  - One serial console
- BIOS Chip: Up to 1 MB onboard Boot and 1 MB Recovery Boot Flash (SPI)
- Onboard storage support
  - 2.5 Inch SATA HDD
  - SATA Cube (SSD): 16, 32, 64, 128 GB capacity
  - USB flash (EUSB SDD), 1, 2 or 4 GB capacity
- Onboard IPMC (IPMI management controller) implements IPMI version 1.5
- Onboard Glue Logic FPGA for IPMC extension and onboard Control register

1.2 Standard Compliances

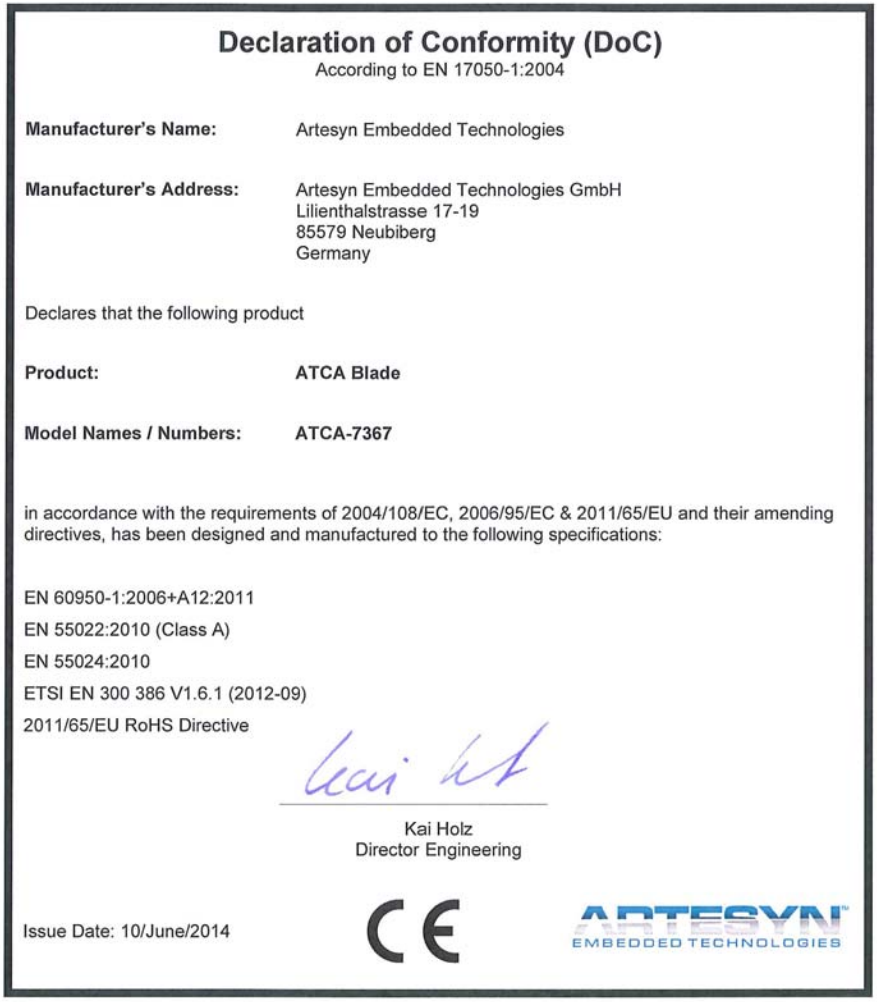
The product is designed to meet the following standards.

Table 1-1 Standard Compliances

Standard	Description
SN29500/8,	Reliability requirements
MIL-HDBK-217F,	
GR-332,	
TR-NWT-000357	
IEC 60068-2-1/2/3/13/14	Climatic environmental requirements. The product can only be used in a restricted temperature range. See section 3.15.2 "Preplacement" on page 31.
IEC 60068-2-27/32/35	Mechanical environmental requirements
EN 60950/UL 60950 (in predefined Force system)	Legal requirements, safety
UL 94V-0/1, Oxygen index for PCBs below 28%	Flammability
EN 55022,	EMC requirements on system level Attention: ATCA boards require CISPR 22 Class B on conducted emissions EMC immunity requirements industrial EMC for telecom equipment
EN 55024,	
EN 61000-6-2,	
EN 300386	
FCC Part 15 Class A	
ANSI/IPC-A-610 Rev.B Class 2,	Manufacturing requirements
ANSI/IPC-R-700B, ANSI-J-001...003	
ISO 8601	Y2K compliance
NEBS Standard GR-63-CORE,	NEBS level three
NEBS Standard GR-1089 CORE	Project is designed to support NEBS level three. The compliance tests must be done with the customer target system.

The product has been designed to meet the directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS) Directive 2002/95/EC.

Figure 1-1 Declaration of Conformity



Declaration of Conformity (DoC)

According to EN 17050-1:2004

Manufacturer's Name: Artesyn Embedded Technologies

Manufacturer's Address: Artesyn Embedded Technologies GmbH
Lilienthalstrasse 17-19
85579 Neubiberg
Germany

Declares that the following product

Product: **ATCA Blade**

Model Names / Numbers: **ATCA-7367**

in accordance with the requirements of 2004/108/EC, 2006/95/EC & 2011/65/EU and their amending directives, has been designed and manufactured to the following specifications:

EN 60950-1:2006+A12:2011
EN 55022:2010 (Class A)
EN 55024:2010
ETSI EN 300 386 V1.6.1 (2012-09)
2011/65/EU RoHS Directive

Kai Holz
Director Engineering

Issue Date: 10/June/2014

CE

ARTESYN EMBEDDED TECHNOLOGIES

1.3 Mechanical Data

The following table provides details about the blade's mechanical data, such as dimensions and weight.

Table 1-2 Mechanical Data

Feature	Value
Dimensions (width x height x depth)	Single slot ATCA 280mm x 322mm
Weight of blade	ATCA-7367-0GB: 3.07 kg ATCA-7367-12GB: 3.15 kg

1.4 Ordering Information

As of the printing date of this manual, this guide supports the models listed below.

Table 1-3 Blade Variants - Ordering Information

Product Name	Description
ATCA-7367-12GB	ATCA processor blade, L5638 6-core (2.0 GHz), 3X 4GB, 10G support, AMC site.[1]
ATCA-7367-24GB	ATCA processor blade, L5638 6-core (2.0 GHz), 3X 8GB, 10G support, AMC site.[1]
ATCA-7367-0GB	ATCA processor blade, L5638 6-core (2.0 GHz), 0GB, 10G support, AMC site.[1,2]
ATCA-7367-12GB-LS	ATCA processor blade, L5638 6-core (2.0 GHz), 3X 4GB, 10G support, on-board SATA drive, no AMC site
ATCA-7367-0GB-LS	ATCA processor blade, L5638 6-core (2.0 GHz), 0GB, 10G support, optional on-board SATA drive, no AMC site.[2]

1. AMC filler panel not included

2. No memory installed

As of the printing date of this manual, the following board accessories are available.

Table 1-4 Blade Accessories - Ordering Information

Accessory	Description
ATCA7367-HDD1-SATA	80GB SATA HDD (ext. temp.) kit for on-board use with ATCA-7367-xxGB-LS
ATCA-7360-MEM-2G	2GB DDR3 VLP memory module for ATCA-736X product series
ATCA-7360-MEM-4G	4GB DDR3 VLP memory module for ATCA-736X product series
ATCA-7360-MEM-8G	8GB DDR3 VLP memory module for ATCA-736X product series
RTM-ATCA-7360	RTM for the ATCA-736X product series, 6X GbE, 2X SAS,1X slot for optional HDD
RTM-ATCA-7360-L	RTM for the ATCA-736X product series, 2X GbE, 2X SAS, 1X slot for optional HDD
ATCA7360-HDD1-SAS	147GB SAS HDD for the RTM-ATCA-7360.[1]
ATCA7360-HDD2-SAS	300GB SAS HDD for the RTM-ATCA-7360.[1]
ATCA7360-HDD3-SATA	80GB SATA HDD (ext. temp.) for the RTM-ATCA-7360.[1]
RTM-ATCA-7360-FC	RTM for the ATCA-736X product series, 6X GBE, 2X SAS, 2X FC.[2]
ATCA7360-MMOD-SATA1	32GB on-board solid state disk at SATA for ATCA-736X product series.[3]
ATCA7360-MMOD-SATA2	64GB on-board solid state disk at SATA for ATCA-736X product series.[3]
ATCA7360-SFMMOD	Reset persistent memory, 16MB SRAM, 64MB flash for the ATCA-736X product series.
AMC-FILLER-MS	AMC filler panel mid-size for ATCA-F12X, ATCA-F140 and ATCA-7367
RJ45-DSUB-ATCA7140	RJ-45 DSUB cable for the ATCA-7140, 7150, 7350, 736X
SA-BBS-WR30-7367	CD - BBS SW and WR PNE 3.0 for ATCA-7367

1. HDD kit option for RTM-ATCA-7360 and RTM-ATCA-7360-L

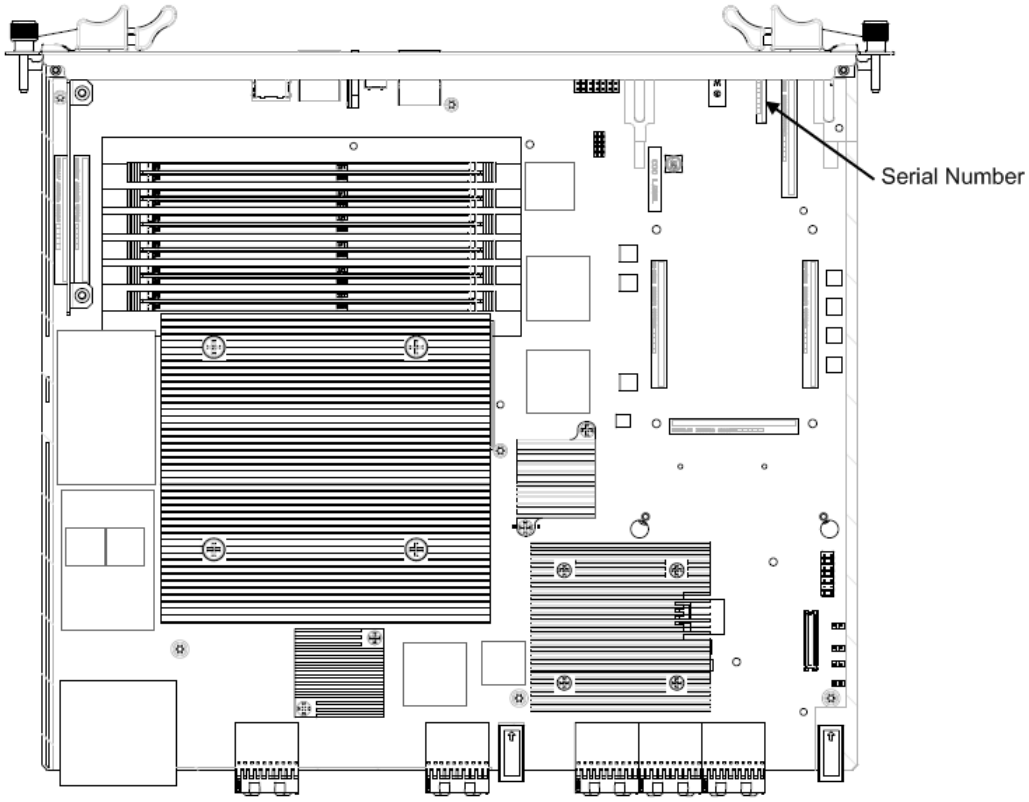
2. RoHS 5/6 (lead exemption)

3. Persistent memory and solid state disk mutually exclusive

1.5 Product Identification

The following graphics shows the location of the serial number label.

Figure 1-2 Serial Number Location



2.1 Unpacking and Inspecting the Blade

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Shipment Inspection

To inspect the shipment, perform the following steps.

1. Verify that you have received all items of your shipment:
   - Printed *Quick Start Guide* and *Safety Notes Summary*
   - ATCA-7367 blade
   - Any optional items ordered
2. Check for damage and report any damage or differences to the customer service.
3. Remove the desiccant bag shipped together with the blade and dispose of it according to your country's legislation.

The blade is thoroughly inspected before shipment. If any damage occurred during transportation or any items are missing, please contact our customer's service immediately.

2.2 Environmental and Power Requirements

In order to meet the environmental requirements, the blade has to be tested in the system in which it is to be installed.

Before you power up the blade, calculate the power needed according to your combination of blade upgrades and accessories.

2.2.1 Environmental Requirements

The environmental conditions must be tested and proven in the shelf configuration used. The conditions refer to the surrounding of the blade within the user environment.

Table 2-1 Environmental Requirements

Requirement	Operating	Non-Operating
Temperature	Normal Operation: +5 °C (41 °F) to +40 °C (104 °F) according to Telcordia GR-63-CORE (NEBS) and ETSI EN 300 019-1-3, Class 3.1 Exceptional Operation: -5 °C (23 °F) to +55 °C (131 °F) according to Telcordia GR-63-CORE (NEBS) Note: This exceeds ETSI EN 300 019-1-3, Class 3.1E requirements (-5°C to +45°C)	-40 °C (-40 °F) to +70 °C (158 °F) according to Telcordia GR-63-CORE (NEBS) and ETSI EN 300 019-1-2, Class 2.3 Note: This exceeds ETSI EN 300 019-1-1, Class 1.2 requirements (storage from -25 °C to +55 °C Note: This may be further limited by installed accessories.
Temp. Change	+/- 0.25 °C/min according to Telcordia GR-63-CORE	+/- 0.25 °C/min
Rel. Humidity	Normal Operation: 5%rH to 85%rh non-condensing Exceptional Operation: 5%rH to 90%rh non-condensing According to Telcordia GR-63-CORE (NEBS) and EN 300 019-1-3, Classes 3.1 and 3.1E	5% to 95% non-condensing according to Telcordia GR-63-CORE (NEBS) and EN 300 019-1-1, Classes 1.2 and 2.3

Table 2-1 Environmental Requirements (continued)

Requirement	Operating	Non-Operating
Vibration	1g from 5 to 200Hz and back to 5Hz at a rate of 0.25 octave/minute (according to Telcordia GR-63-core)	5-20 Hz at 0.01 g^2/Hz (according to Telcordia GR-63-core and ETSI EN 300 019-2-2) 20-200 Hz at -3 dB/octave Hz (according to Telcordia GR-63-core and ETSI EN 300 019-2-2) Random 5-20Hz at 1 m^2/s^3 Random 20-200Hz at 3 m^2/s^3
Shock	Half-sine, 11 ms, 30 m/s^2	Blade level packaging Half-sine, 6 ms at 180 m/s^2
Free Fall	-	1.2 m/ packaged (according to ETSI 300 019-2-2) 100 mm unpackaged (according to Telcordia GR-63-core)

- The environmental requirements of the blade may be further limited down due to installed accessories, such as hard disks or AMC modules, with more restrictive environmental requirements.
- Operating temperatures refer to the temperature of the air circulating around the blade and not to the actual component temperature.

NOTICE

Blade Damage
Blade Surface
High humidity and condensation on the blade surface causes short circuits.
Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power.

Blade Overheating and Blade Damage
Operating the blade without forced air cooling may lead to blade overheating and thus blade damage.
When operating the blade, make sure that forced air cooling is available on the shelf.

2.2.2 Power Requirements

The blade's power requirements depend on the installed hardware accessories. If you want to install accessories on the blade, the load of the respective accessory has to be added to that of the blade. In the following table you will find typical examples of power requirements with and without accessories installed. For information on the accessories' power requirements, refer to the documentation delivered together with the respective accessory or consult your local Artesyn Embedded Technologies representative for further details.

The blade must be connected to a TNV-2 or a safety-extra-low-voltage (SELV) circuit. A TNV-2 circuit is a circuit whose normal operating voltages exceed the limits for a SELV circuit under normal operating conditions, and which is not subject to over voltages from telecommunication networks.

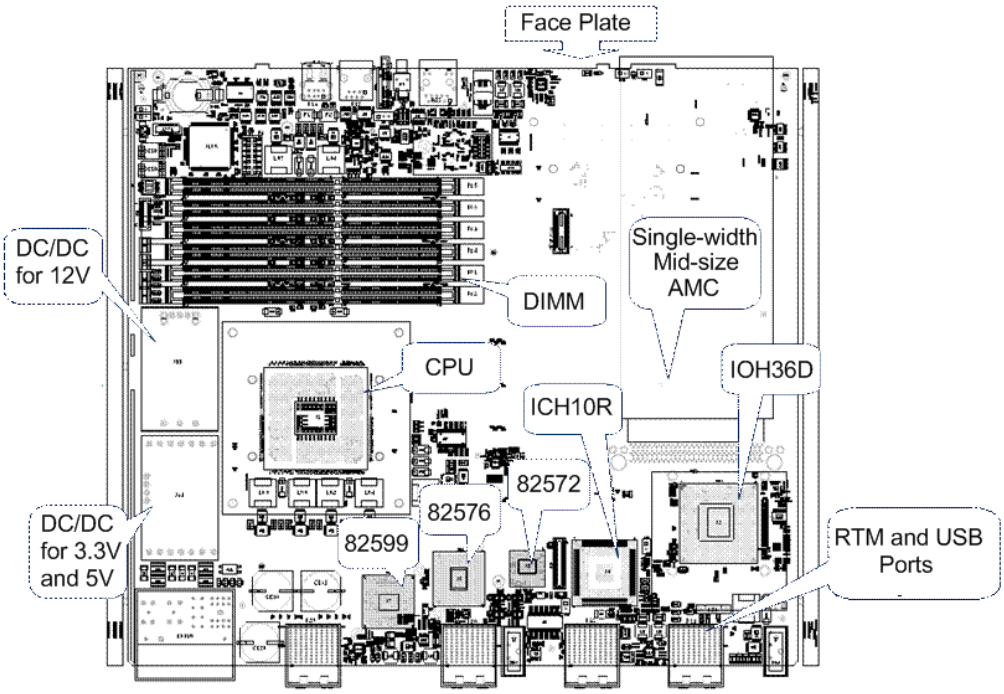
Table 2-2 Power Requirements

Characteristic	Value
Max. power consumption of ATCA-7367 (No power limit)	152 W
Max. power consumption of ATCA-7367 (P-states limited)	116 W

2.3 Blade Layout

The following figure shows the location of components on the ATCA-7367:

Figure 2-1 ATCA-7367 Blade Layout



2.4 Switch Settings

All mechanical switches are OFF in their default configuration. Switch selection used for debugging is grouped in separate devices. These devices are not assembled in volume production.Switches reside on the component side 1 and are not covered by any other component.

NOTICE

Blade Malfunction
Switches marked as "Reserved" may carry production-related functions and may cause the blade to malfunction if the setting is changed.
Therefore, do not change settings of switches marked as "Reserved". The setting of switches which are not marked as "Reserved" has to be checked and changed before blade installation.

Blade Damage
Setting/resetting the switches during operation can cause blade damage.
Therefore, check and change switch settings before you install the blade.

For normal operation, all switches must be OFF. Switches are used only for repair, manual maintenance and critical crisis recovery. For remote maintenance and in order that all firmware upgrade features through IPMC are available, all switches must be in their default OFF position and are controlled through IPMC.

Table 2-3 Switch SW1 settings

Switch	Function	Default	
SW1.1	Default SPI Boot Flash Write protection	OFF	Not Write Protected
SW1.2	Recovery SPI Boot Flash Write protection	OFF	Not Write Protected

Table 2-3 Switch SW1 settings (continued)

Switch	Function	Default	
SW1.3	TSOP or Debug-Socket SPI Boot select OFF= boot from TSOP SPI Flash (either Default/Recovery) ON = boot from Debug Socket SPI Flash	OFF	Boot from TSOP SPI Flash
SW1.4	ICH10 GPIO33-Pinstrap: SPI Flash Descriptor Security Override Strap and ME disable if sampled LOW	OFF	No SPI Flash Descriptor security override and ME working in S0/S1

Table 2-4 Switch SW2 Settings

Switch	Function	Default	
SW2.2	SW2.2 IPMC Debug Console Routing OFF - IPMC Debug Console at 3-pin Header ON - IPMC Debug Console at Faceplate instead of FPGA COM	OFF/OFF	IPMC Debug Console (TTL-level) routing OFF:IPMC Debug Console at 3-pin Header

Table 2-5 Switch SW3 Settings

Switch	Function	Default	
SW3.1	Enable manual "Default SPI Boot Flash" / "Recovery SPI Boot Flash" selection . OFF: Boot Bank controlled by IPMI (default) ON: Boot bank controlled by SW3.2	OFF	IPMI selects Boot Flash
SW3.2	SW3.2 controls Boot flash selection if SW3.1 is set to ON. OFF: Booting from Boot Bank A ON: Booting from Boot Bank B	OFF	

Table 2-5 Switch SW3 Settings (continued)

Switch	Function	Default	
SW3.3	OFF = Reset push button enabled ON = Reset push button disabled	OFF	Disable face plate reset push button

Table 2-6 Switch SW4 Settings

Switch	Function	Default	
SW4.1	Top-block Swap configuration OFF = enabled (GP[55]/GNT3#] pin strap internal Pull-up) ON = disable Top Swap	OFF	Top Swap enabled
SW4.2	TCO timer timeout reboot mode (Speaker Pin strap) OFF = enable (SPKR input internal Pull-down) ON = disabled	OFF	TCO Reboot Timer enabled
SW4.3	Load BIOS Defaults OFF= load BIOS Defaults if SW4-4 ON ON= Port80 to COM1	OFF	[SW4.4, SW4.3] 00 - Normal operation, 01- Load Bios Defaults, 10 - Crisis recovery, 11- Pot80 to COM1
SW4.4	BIOS Crisis Recovery OFF = BIOS Crisis Recovery if SW4-3 ON	OFF	

2.5 Installing the Blade Accessories

The following additional components are available for the blade:

- DIMM memory modules
- PMEM (persistent memory) module

- SATA module
- USB flash module
- Rear transition modules
- AMC module

They are described in detail in the following sections. For order numbers refer to section *Ordering Information* on page 39.

2.5.1 DIMM Memory Modules

The blade provides six memory slots for main memory DIMM modules. You may install and/or remove DIMM memory modules in order to adapt the main memory size to your needs. The corresponding installation/removal procedures are described in this section.

The location of the DIMM Memory Modules are shown in Figure "ATCA-7367 Blade Layout" on page 47.

When installing DIMM memory modules, the DIMM sockets farthest away on each memory channel from the CPU device need to be populated first. Only qualified DDR3 DIMMs (Dual Ranked RDIMM) are allowed.

ATCA-7367 supports low-voltage DDR3 memory. This is available upon request.

DIMM modules used within one channel must be based on the same memory technology. For maximum memory performance all three channels of one CPU must be equipped with an identical amount and size of DIMMs.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

Installation Procedure

To install a DIMM module, proceed as follows:

1. Remove blade from system as described in *Installing and Removing the Blade* on page 56.
2. Open locks of memory module socket.
3. Press module carefully into socket.
   As soon as the memory module has been fully inserted, the locks automatically close.
4. If applicable, repeat steps 2 to 3 to install further modules.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

Removal Procedure

To remove a DIMM module, proceed as follows:

1. Remove blade from system as described in *Installing and Removing the Blade* on page 56.
2. Open locks of socket at both sides.
   The memory module is automatically lifted up.
3. Remove module from socket.
4. Repeat steps 2 to 3 in order to remove further memory modules.

2.5.2 PMEM and SATA Module

The PMEM/SATA extension slot allows assembly of either a PMEM or SATA module which are available as upgrade kits for ATCA-7367. PMEM module consists of an SRAM and a flash memory. The SRAM has a capacity of up to 16 MB and can be used as persistent memory, i.e. a memory that holds up the contents during reset. The flash memory has a capacity of up to 64 MB organized as two memory banks. The S/F memory module connects to the blade's PCI subsystem. It can be configured via an FPGA register.

The SATA module consists of a Solid State Disc of up to 128 GB and a SATA controller and connects physically to ICH10 SATA Port #5.

The extension module is mechanically fastened to the blade with two screws. The location of the two corresponding mounting holes as well as the S/F memory module connector is shown in Figure "ATCA-7367 Blade Layout" on page 47.

The PMEM and SATA module are accessory kits and are not part of the default ATCA-7367. The following procedure describes the steps to install/remove the PMEM/SATA module.

Installation Procedure

To install a PMEM/SATA module, proceed as follows:

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

1. Remove the blade from the system as described in *Installing and Removing the Blade* on page 56.
2. Plug the PMEM/SATA module on the blade so that the module's standoffs fit in the blade's mounting holes.
3. Fasten the PMEM/SATA module to the blade using the two screws that previously had fixed the S/F memory module to the blade.
4. Reinstall the blade into the system as described in *Installing and Removing the Blade* on page 56.
   The additional resource (either memory or SATA SSD) will be detected automatically during the boot-up sequence.

Removal Procedure

To remove a PMEM/SATA module, proceed as follows:

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

1. Remove the blade from the system as described in *Installing and Removing the Blade* on page 56.
2. Remove the two screws holding the PMEM/SATA module.
3. Remove the PMEM/SATA module from the blade.
4. Reinstall the blade into the system as described in *Installing and Removing the Blade* on page 56.

2.5.3 USB 2.0 Flash Module

The blades provides a USB 2.0 flash module with a capacity of 4 GB or 16 GB. The corresponding removal/installation procedures are described in this section.

The location of the USB 2.0 Flash Module is shown in Figure "ATCA-7367 Blade Layout" on page 47.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

Removal Procedure

To remove a USB flash module, proceed as follows:

1. Remove blade from system as described in *Removing the Blade* on page 60.
2. Remove the screw on the left side of the flash module (see figure Figure 2-1 on page 47).
3. Lift the flash module from the socket.

Installation Procedure

To install a USB flash module, proceed as follows:

1. Remove blade from system as described in *Removing the Blade* on page 60.
2. Insert new flash module in socket (see figure Figure 2-1 on page 47).
3. Tighten the screw on the left side of the flash module.

2.6 Installing and Removing the Blade

The blade is fully compatible to the AdvancedTCA standard and is designed to be used in AdvancedTCA shelves.

The blade can be installed in any AdvancedTCA node slot. Do not install it in an AdvancedTCA hub slot.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Blade Malfunctioning
Incorrect blade installation and removal can result in blade malfunctioning.
When plugging the blade in or removing it, do not press on the face plate but use the handles.

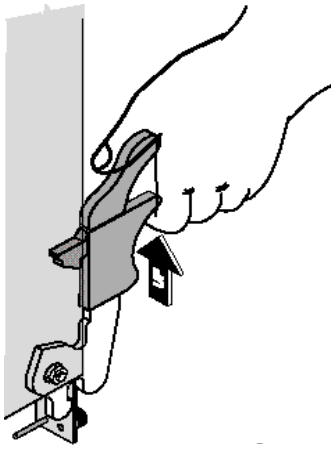
2.6.1 Installing the Blade

To install the blade into an AdvancedTCA shelf, proceed as follows.

Installation Procedure

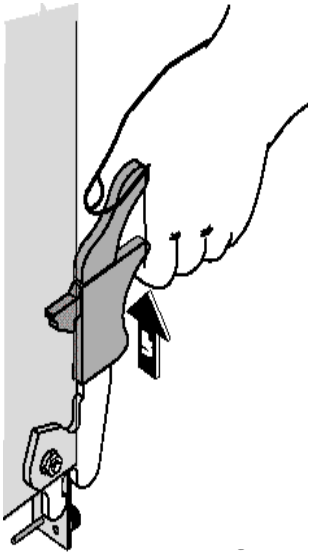
The following procedure describes the installation of the blade. It assumes that your system is powered on. If your system is not powered on, you can disregard the blue LED and thus skip the respective step. In this case, it is purely a mechanical installation.

1. Ensure that the top and bottom ejector handles are in the outward position by squeezing the lever and the latch together.



2. Insert blade into the shelf by placing the top and bottom edges of the blade in the card guides of the shelf. Ensure that the guiding module of shelf and blade are aligned properly.
3. Apply equal and steady pressure to the blade to carefully slide the blade into the shelf until you feel resistance. Continue to gently push the blade until the blade connectors engage.
4. Squeeze the lever and the latch together and hook the lower and the upper handle into the shelf rail recesses.

5. Fully insert the blade and lock it to the shelf by squeezing the lever and the latch together and turning the handles towards the face plate.



If your shelf is powered on, as soon as the blade is connected to the backplane power pins, the blue LED is illuminated.
When the blade is completely installed, the blue LED starts to blink. This indicates that the blade announces its presence to the shelf management controller.

If an RTM is connected to the front blade, make sure that the handles of both the RTM and the front blade are closed in order to power up the blade's payload.

6. Wait until the blue LED is switched off, then tighten the face plate screws which secure the blade to the shelf.
   The switched off blue LED indicates that the blade's payload has been powered up and that the blade is active.

7. Connect cables to the face plate, if applicable.

2.6.2 Removing the Blade

This section describes how to remove the blade from an AdvancedTCA system.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Blade Malfunctioning
Incorrect blade installation and removal can result in blade malfunctioning.
When plugging the blade in or removing it, do not press on the face plate but use the handles.

Removal Procedure

The following procedure describes how to remove the blade from a system. It assumes that the system is powered on. If the system is not powered on, you can disregards the blue LED and thus skip the respective step. In that case, it is a purely a mechanical procedure.

1. Unlatch the lower handle by squeezing the lever and the latch together and turning the handle outward just enough to unlatch the handle from the face plate. Do not rotate the handle fully outward.
   The blue LED blinks indicating that the blade power-down process is ongoing.
2. Wait until the blue LED is illuminated permanently, then unlatch the upper handle and rotate both handles fully outward.

If the LED continues to blink, a possible reason may be that the upper layer software rejected the blade extraction request.

NOTICE

Data Loss
Removing the blade with the blue LED still blinking causes data loss.
Wait until the blue LED is permanently illuminated, before removing the blade.

3. Remove the face plate cables, if applicable.
4. Unfasten the screws of the face plate until the blade is detached from the shelf.
5. Remove the blade from the shelf.

3.1 Mechanical Layout

The following graphics illustrate the mechanical layout of the blade.

Figure 3-1 Mechanical Layout (with AMC)

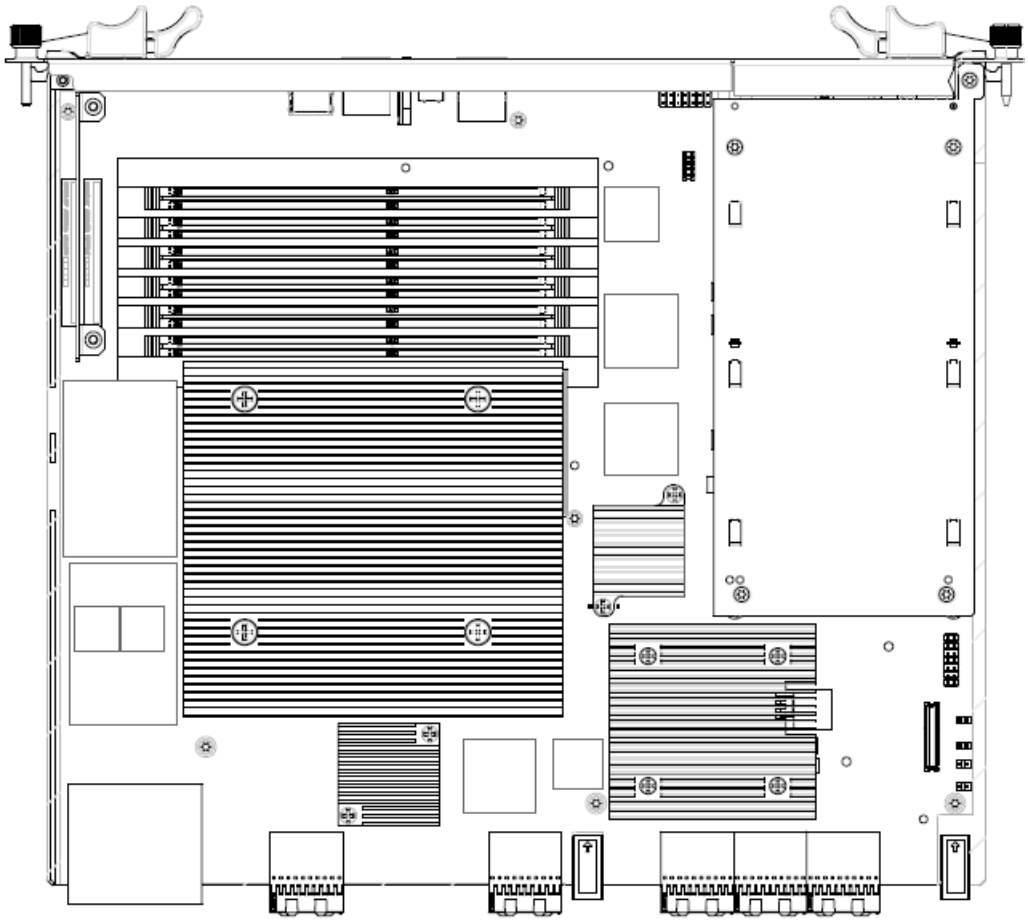


Figure 3-2 Mechanical Layout (without AMC and HDD)

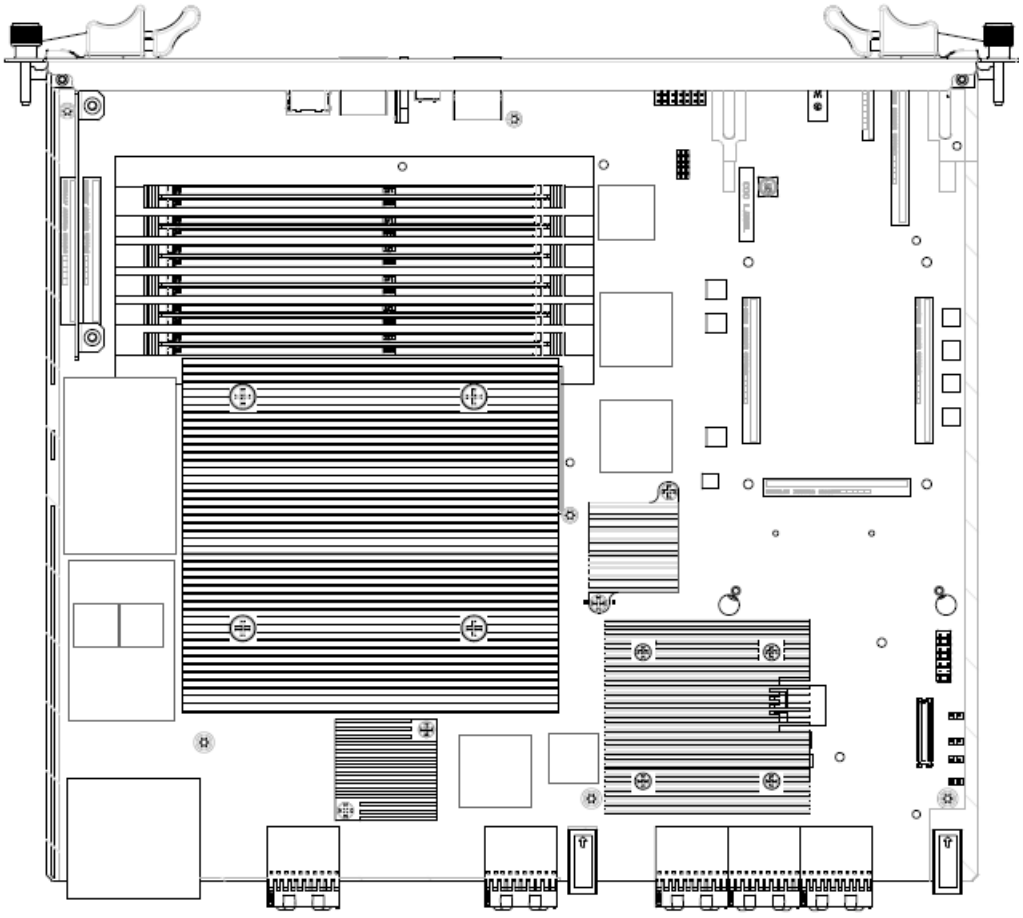
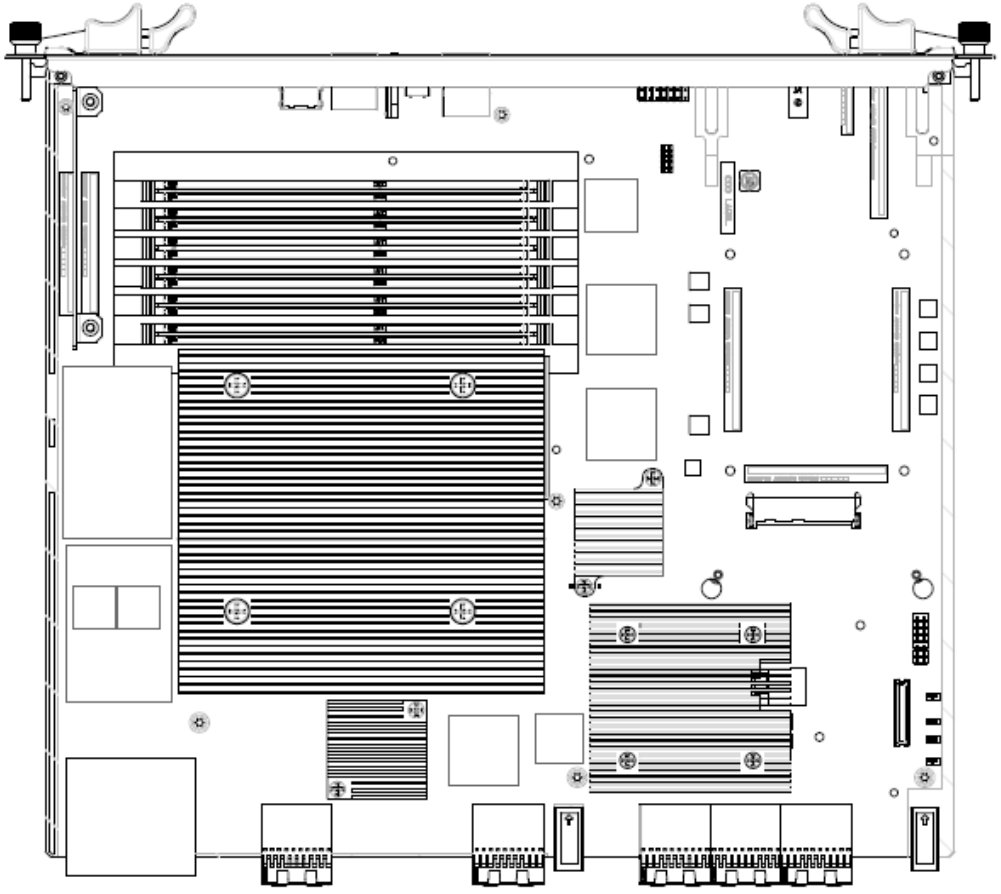


Figure 3-3 Mechanical Layout (without AMC/ with HDD)

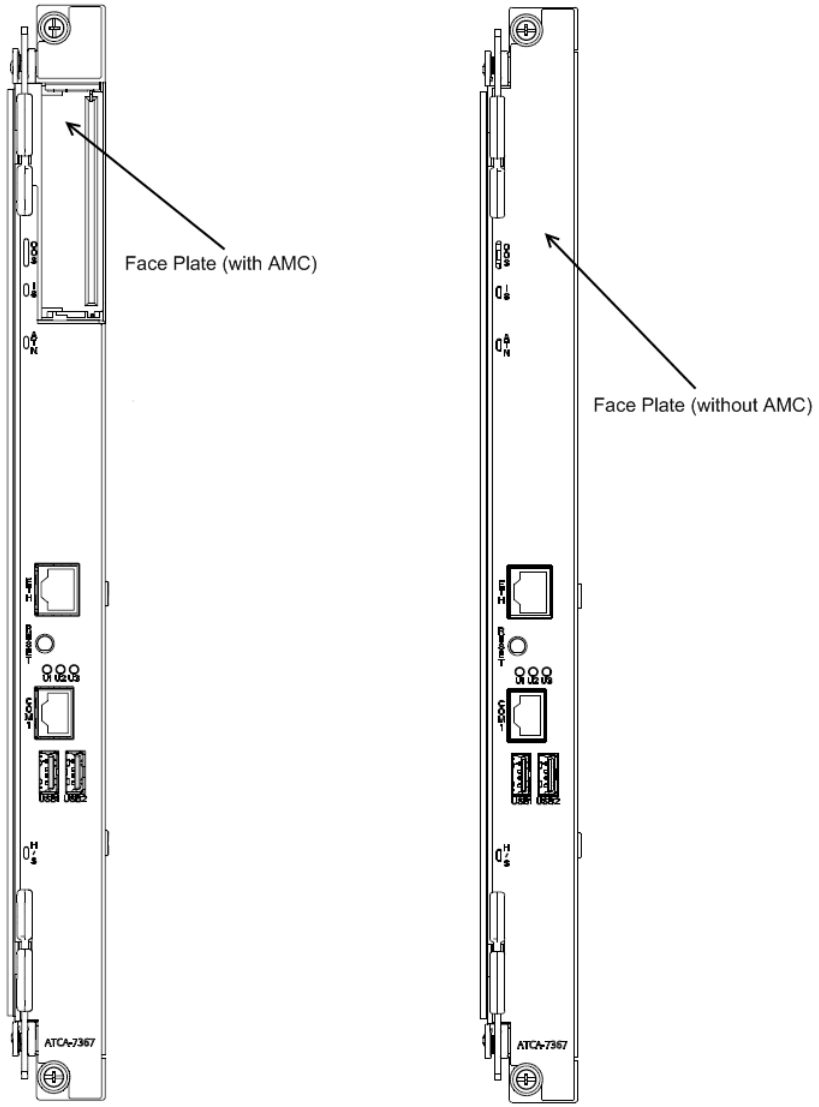


3.2 Face Plate

The following figure shows the connectors, keys and LEDs available at the face plate.

The blade design provides the possibility to cover unused faceplate elements like LEDs or push buttons behind a custom overlay foil. The following figure gives an overview of the ATCA-7367 faceplate features.

Figure 3-4 Face Plates



3.2.1 LEDs

The blade's face plate provides the following interfaces and control elements :

- Two USB 2.0 ports
- Serial console port to connect to either payload or IPMC serial I/F
- Out of Service, In Service, Attention, and Hot Swap LEDs (IPMC control)
- One 1000Base-T Ethernet ports. The Ethernet connector provides two status LEDs.
- LEDs connected to FPGA for BASE IF and Faceplate IF Link Control (FPGA control)
- Recessed reset button

The meaning of these LEDs is described in the following table.

Table 3-1 Face Plate LEDs

LED	Color	Description
OOS	Red	Out Of Service This LED is multicolored (red/amber) and is programmable through IPMC. Its default color is red and its local control state (on or off) reflects the payload power state (on or off). It permits override control by higher layer software, such as middle ware or applications, as specified in PICMG 3.0 specification.
IS	Green	Payload Power Status This LED is multicolored (green/red/amber) and is programmable through IPMC. Its default color is green and its local control state is off. It permits override control by higher layer software, such as middle ware or applications, as specified in PICMG 3.0 specification.
ATN	Amber	Attention This LED has amber color and is programmable through IPMC. Its local control state is off. It permits override control by higher layer software, such as middle ware or applications, as specified in PICMG 3.0 specification.
ETH connector		
ETH Activity	Green	Ethernet Activity Off: No activity

Table 3-1 Face Plate LEDs (continued)

LED	Color	Description
ETH Link	Amber	Ethernet Link established Off: No Link
U1, U2	Red	Base Interface activity is visualized via FPGA LEDs U1 and U2
U3	Alternatively Red/Green/ Amber	User LED, selectable color via FPGA register. Colors: red, green, amber
H/S	Blue	FRU State Machine ● During blade Installation: – Permanently blue: On-board IPMC powers up – Blinking blue: Blade communicates with shelf manager – OFF: Blade is active ● During blade removal: – Blinking blue: Blade notifies shelf manager of its desire to deactivate – Permanently blue: Blade is ready to be extracted

3.2.2 Connectors

3.2.2.1 Face Plate Connectors

Table 3-2 RJ45 female Serial Line Connector Pinout

Pin	Signal
1	NC
2	NC
3	COM1_RS232_TXD
4	GND
5	GND
6	COM1_RS232_RXD
7	NC

Table 3-2 RJ45 female Serial Line Connector Pinout (continued)

Pin	Signal
8	NC

Table 3-3 USB Connector Pinout

Pin	Signal
1	VP5_USB
2	USB_x_D-
3	USB_x_D+
4	GND

Table 3-4 10/100/1000Base-T Fast Ethernet Connector Pinout

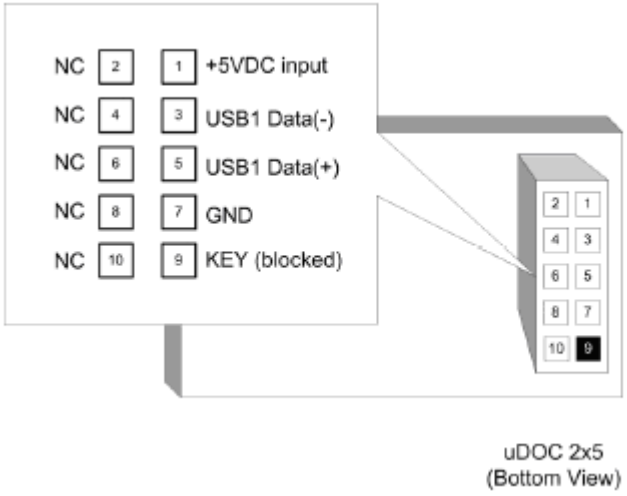
Pin	Name	
1	BI_DA+	Bi-directional pair A +
2	BI_DA-	Bi-directional pair A -
3	BI_DB+	Bi-directional pair B +
4	BI_DC+	Bi-directional pair C +
5	BI_DC-	Bi-directional pair C -
6	BI_DB-	Bi-directional pair B -
7	BI_DD+	Bi-directional pair D +
8	BI_DD-	Bi-directional pair D -

3.3 Onboard Connectors

3.3.1 USB2.0 FLASH Connector

One USB Port of ICH10R is connected to the onboard USB Flash Disk Module.

Figure 3-5 USB2.0 Flash Disk module connector pinout



3.3.2 Keying

Mechanical keying is provided according to ATCA 3.0 base specification.

Table 3-5 Keying

Key	Value
Zone 1/2 A1/K1 Keying	Default "11" Keyed
Zone 3 A2/K2 Keying	synch to RTM

3.3.3 Backplane Connectors

Table 3-6 Zone 1 Connector P1 Pin Assignment

Contact Number	Destination	Description
1 - 4	Reserved	Reserved
5	IPMC ISC PC0	Hardware Address Bit 0
6	IPMC ISC PC1	Hardware Address Bit 1
7	IPMC ISC PC2	Hardware Address Bit 2
8	IPMC ISC PC3	Hardware Address Bit 3
9	IPMC ISC PD4	Hardware Address Bit 4
10	IPMC ISC PD5	Hardware Address Bit 5
11	IPMC ISC PD6	Hardware Address Bit 6
12	IPMC ISC PD7	Hardware Address Bit 7
13	IPMC IMC PD0	IPMB Clock Port A
14	IPMC IMC PD1	IPMB Data Port A
15	IPMC ISC PC5	IPMB Clock Port B
16	IPMC ISC PC4	IPMB Data Port A
17 - 24	Not used	Not used
25	Shelf Ground	Shelf Ground
26	Logic Ground	Logic Ground
27	Power Building Block	Enable B
28	Power Building Block	Voltage Return A
29	Power Building Block	Voltage Return B
30	Power Building Block	Early -48V A
31	Power Building Block	Early -48V B
32	Power Building Block	Enable A
33	Power Building Block	-48V A
34	Power Building Block	-48V A

Table 3-7 Zone 2 Connector P20 Pin Assignment

P20									
Row #	Interface	Col AB		Col CD		Col EF		Col GH	
1	CLKs	CLK1A+	CLK1A-	CLK1B+	CLK1B-	CLK2A+	CLK2A-	CLK2B+	CLK2B-
2	Update Channel	NC	NC	Term	Term	CLK3A+	CLK3A-	CLK3B+	CLK3B-
3		UC[2]_TX+	UC[2]_TX-	UC[2]_RX+	UC[2]_RX-	NC	NC	Term	Term
4		UC[0]_TX+	UC[0]_TX-	UC[0]_RX+	UC[0]_RX-	UC[1]_TX+	UC[1]_TX-	UC[1]_RX+	UC[1]_RX-
5	Fabric Channel 15	NC	NC	Term	Term	NC	NC	Term	Term
6		NC	NC	Term	Term	NC	NC	Term	Term
7	Fabric Channel 14	NC	NC	Term	Term	NC	NC	Term	Term
8		NC	NC	Term	Term	NC	NC	Term	Term
9	Fabric Channel 13	NC	NC	Term	Term	NC	NC	Term	Term
10		NC	NC	Term	Term	NC	NC	Term	Term

Table 3-8 Zone 2 Connector P23 Pin Assignment

P23									
Row #	Interface	Col AB		Col CD		Col EF		Col GH	
1	Fabric Channel 2	F2[2]_TX+	F2[2]_TX-	F2[2]_RX+	F2[2]_RX-	F2[3]_TX+	F2[3]_TX-	F2[3]_RX+	F2[3]_RX-
2		F2[0]_TX+	F2[0]_TX-	F2[0]_RX+	F2[0]_RX-	F2[1]_TX+	F2[1]_TX-	F2[1]_RX+	F2[1]_RX-
3	Fabric Channel 1	F1[2]_TX+	F1[2]_TX-	F1[2]_RX+	F1[2]_RX-	F1[3]_TX+	F1[3]_TX-	F1[3]_RX+	F1[3]_RX-
4		F1[0]_TX+	F1[0]_TX-	F1[0]_RX+	F1[0]_RX-	F1[1]_TX+	F1[1]_TX-	F1[1]_RX+	F1[1]_RX-
5	Base Channel 1	BI1_DA+	BI1_DA-	BI1_DB+	BI1_DB-	BI1_DC+	BI1_DC-	BI1_DD+	BI1_DD-
6	Base Channel 2	BI2_DA+	BI2_DA-	BI2_DB+	BI2_DB-	BI2_DC+	BI2_DC-	BI2_DD+	BI2_DD-

Table 3-8 Zone 2 Connector P23 Pin Assignment (continued)

P23									
7	n/a	NC	NC	NC	NC	NC	NC	NC	NC
8	n/a	NC	NC	NC	NC	NC	NC	NC	NC
9	n/a	NC	NC	NC	NC	NC	NC	NC	NC
10	n/a	NC	NC	NC	NC	NC	NC	NC	NC

3.3.4 Zone 3

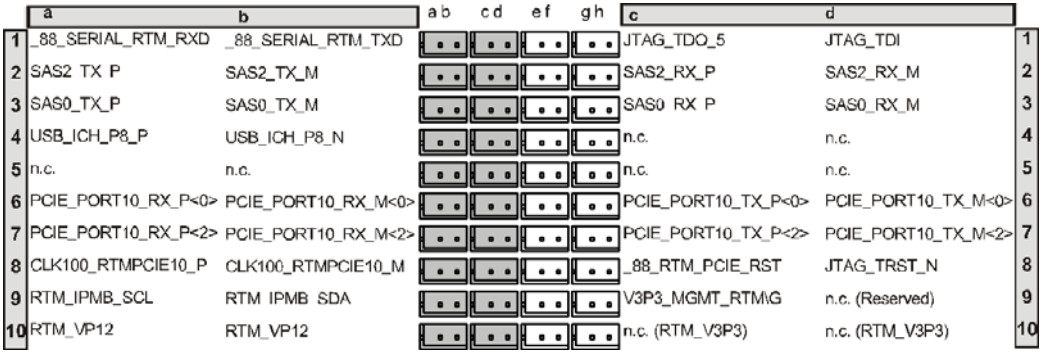
The ATCA specification defines Zone 3 for user input/output signals. On ATCA-7367, ATCA Zone 3 Type A connector (direct connect to RTM) is used. The same connectors are used for Zone 2 and Zone 3. Zone 3 connectors are assigned to reference designators P30 through P32.

Zone 3 contains the two connectors P30 and P32. They are used to connect an RTM to the blade and carry the following signals:

- Serial (RS232_x_yyyy)
- Serial ATA (SATAx_yyy)
- USB (USBxy)
- PCI Express (PCIEx_yyy)
- IPMI (IPMB1_xxx, ISMB_xxx)
- Power (VP12_RTM, V3P3_RTM, VP5_RTM)

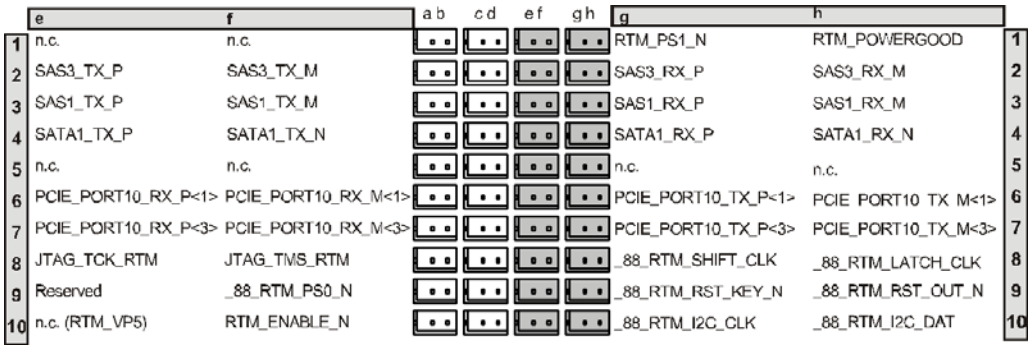
- SAS Update channels
- General control signals (BD_PRESENTx, RTM_PRSNT_N, RTM_RST_KEY-, RTM_RST-)

Figure 3-6 P30 Backplane Connector Pinout - Rows A to D



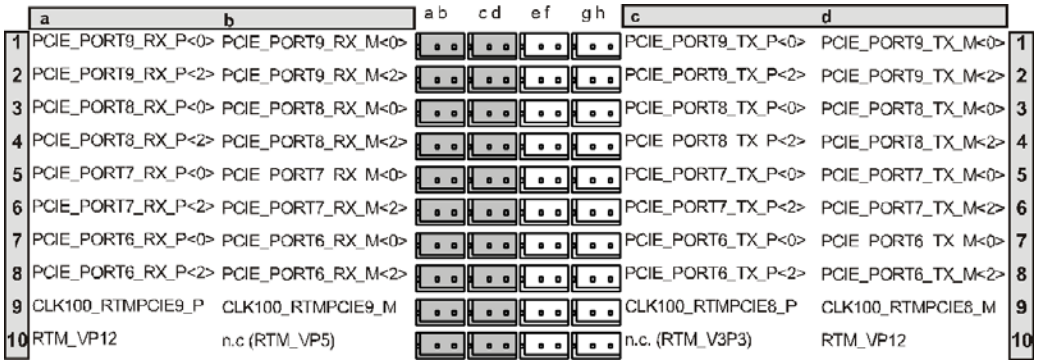
	a	b	ab	cd	ef	gh	c	d	
1	_88_SERIAL_RTM_RXD	_88_SERIAL_RTM_TXD					JTAG_TDO_5	JTAG_TDI	1
2	SAS2_TX_P	SAS2_TX_M					SAS2_RX_P	SAS2_RX_M	2
3	SAS0_TX_P	SAS0_TX_M					SAS0_RX_P	SAS0_RX_M	3
4	USB_ICH_P8_P	USB_ICH_P8_N					n.c.	n.c.	4
5	n.c.	n.c.					n.c.	n.c.	5
6	PCIE_PORT10_RX_P<0>	PCIE_PORT10_RX_M<0>					PCIE_PORT10_TX_P<0>	PCIE_PORT10_TX_M<0>	6
7	PCIE_PORT10_RX_P<2>	PCIE_PORT10_RX_M<2>					PCIE_PORT10_TX_P<2>	PCIE_PORT10_TX_M<2>	7
8	CLK100_RTMPCIE10_P	CLK100_RTMPCIE10_M					_88_RTM_PCIE_RST	JTAG_TRST_N	8
9	RTM_IPMB_SCL	RTM_IPMB_SDA					V3P3_MGMT_RTM\G	n.c. (Reserved)	9
10	RTM_VP12	RTM_VP12					n.c. (RTM_V3P3)	n.c. (RTM_V3P3)	10

Figure 3-7 P30 Backplane Connector Pinout - Rows E to H -



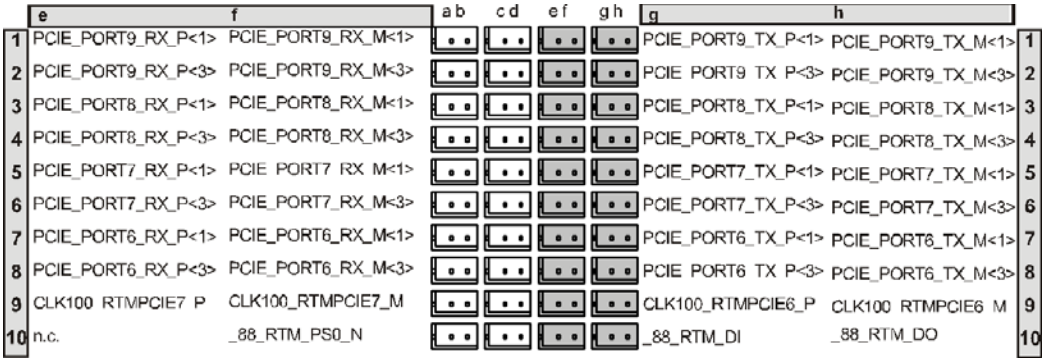
	e	f	ab	cd	ef	gh	g	h	
1	n.c.	n.c.					RTM_PS1_N	RTM_POWERGOOD	1
2	SAS3_TX_P	SAS3_TX_M					SAS3_RX_P	SAS3_RX_M	2
3	SAS1_TX_P	SAS1_TX_M					SAS1_RX_P	SAS1_RX_M	3
4	SATA1_TX_P	SATA1_TX_N					SATA1_RX_P	SATA1_RX_N	4
5	n.c.	n.c.					n.c.	n.c.	5
6	PCIE_PORT10_RX_P<1>	PCIE_PORT10_RX_M<1>					PCIE_PORT10_TX_P<1>	PCIE_PORT10_TX_M<1>	6
7	PCIE_PORT10_RX_P<3>	PCIE_PORT10_RX_M<3>					PCIE_PORT10_TX_P<3>	PCIE_PORT10_TX_M<3>	7
8	JTAG_TCK_RTM	JTAG_TMS_RTM					_88_RTM_SHIFT_CLK	_88_RTM_LATCH_CLK	8
9	Reserved	_88_RTM_PS0_N					_88_RTM_RST_KEY_N	_88_RTM_RST_OUT_N	9
10	n.c. (RTM_VP5)	RTM_ENABLE_N					_88_RTM_I2C_CLK	_88_RTM_I2C_DAT	10

Figure 3-8 P32 Backplane Connector Pinout - Rows A to D -



	a	b	ab	cd	ef	gh	c	d	
1	PCIE_PORT9_RX_P<0>	PCIE_PORT9_RX_M<0>					PCIE_PORT9_TX_P<0>	PCIE_PORT9_TX_M<0>	1
2	PCIE_PORT9_RX_P<2>	PCIE_PORT9_RX_M<2>					PCIE_PORT9_TX_P<2>	PCIE_PORT9_TX_M<2>	2
3	PCIE_PORT8_RX_P<0>	PCIE_PORT8_RX_M<0>					PCIE_PORT8_TX_P<0>	PCIE_PORT8_TX_M<0>	3
4	PCIE_PORT8_RX_P<2>	PCIE_PORT8_RX_M<2>					PCIE_PORT8_TX_P<2>	PCIE_PORT8_TX_M<2>	4
5	PCIE_PORT7_RX_P<0>	PCIE_PORT7_RX_M<0>					PCIE_PORT7_TX_P<0>	PCIE_PORT7_TX_M<0>	5
6	PCIE_PORT7_RX_P<2>	PCIE_PORT7_RX_M<2>					PCIE_PORT7_TX_P<2>	PCIE_PORT7_TX_M<2>	6
7	PCIE_PORT6_RX_P<0>	PCIE_PORT6_RX_M<0>					PCIE_PORT6_TX_P<0>	PCIE_PORT6_TX_M<0>	7
8	PCIE_PORT6_RX_P<2>	PCIE_PORT6_RX_M<2>					PCIE_PORT6_TX_P<2>	PCIE_PORT6_TX_M<2>	8
9	CLK100_RTMPCIE9_P	CLK100_RTMPCIE9_M					CLK100_RTMPCIE8_P	CLK100_RTMPCIE8_M	9
10	RTM_VP12	n.c (RTM_VP5)					n.c. (RTM_V3P3)	RTM_VP12	10

Figure 3-9 P32 Backplane Connector Pinout - Rows E to H -



	e	f	ab	cd	ef	gh	g	h	
1	PCIE_PORT9_RX_P<1>	PCIE_PORT9_RX_M<1>					PCIE_PORT9_TX_P<1>	PCIE_PORT9_TX_M<1>	1
2	PCIE_PORT9_RX_P<3>	PCIE_PORT9_RX_M<3>					PCIE_PORT9_TX_P<3>	PCIE_PORT9_TX_M<3>	2
3	PCIE_PORT8_RX_P<1>	PCIE_PORT8_RX_M<1>					PCIE_PORT8_TX_P<1>	PCIE_PORT8_TX_M<1>	3
4	PCIE_PORT8_RX_P<3>	PCIE_PORT8_RX_M<3>					PCIE_PORT8_TX_P<3>	PCIE_PORT8_TX_M<3>	4
5	PCIE_PORT7_RX_P<1>	PCIE_PORT7_RX_M<1>					PCIE_PORT7_TX_P<1>	PCIE_PORT7_TX_M<1>	5
6	PCIE_PORT7_RX_P<3>	PCIE_PORT7_RX_M<3>					PCIE_PORT7_TX_P<3>	PCIE_PORT7_TX_M<3>	6
7	PCIE_PORT6_RX_P<1>	PCIE_PORT6_RX_M<1>					PCIE_PORT6_TX_P<1>	PCIE_PORT6_TX_M<1>	7
8	PCIE_PORT6_RX_P<3>	PCIE_PORT6_RX_M<3>					PCIE_PORT6_TX_P<3>	PCIE_PORT6_TX_M<3>	8
9	CLK100_RTMPCIE7_P	CLK100_RTMPCIE7_M					CLK100_RTMPCIE6_P	CLK100_RTMPCIE6_M	9
10	n.c.	_88_RTM_PS0_N					_88_RTM_DI	_88_RTM_DO	10

4.1 Introduction

The Basic Input Output System (BIOS) provides an interface between the operating system and the hardware of the blade. It is used for hardware configuration. Before loading the operating system, BIOS performs basic hardware tests and prepares the blade for the initial boot-up procedure.

During blade production, identical BIOS images are programmed into both boot flash banks. It is possible to select boot flash as device to boot from. This is done via an IPMI command. For further details refer to section *Supported IPMI Commands* on page 145.

The BIOS used on the blade is based on the AMI UEFI BIOS with several Artesyn Embedded Technologies extensions integrated. Its main features are:

- Initialize CPU, chipset and memory
- Initialize PCI devices
- Setup utility for setting configuration data
- IPMC support
- Serial console redirection for remote blade access
- Boot operation system

The BIOS complies with the following specifications:

- UEFI Specification 2.0
- Plug and Play BIOS Specification 1.0A
- PCI BIOS Specification 2.1
- SMBIOS Specification 2.3
- BIOS Boot Specification 1.01
- PXE 2.1

- SMP 1.4
- ACPI 3.0b

The BIOS contains online documentation which describes in detail the available menu options. Therefore, the description in this manual is limited to the main BIOS functions.

The BIOS setup program is required to configure the blade hardware. This configuration is necessary for operating the blade and connected peripherals. The configuration data are stored in the same flash device from which the board boots.

When you are not sure about configuration settings, restore the default values. This option is provided in case a value has been changed and you wish to reset settings. To restore the default values, press <F3> in Setup.

- Loading the BIOS default values will affect all set-up items and will reset options previously altered.
- If you set the default values, the displayed default values takes effect only after the BIOS setup is saved and closed.

4.2 Accessing the Blade using the Serial Console Redirection

The blade firmware provides a serial console redirection feature allowing remote access to the blade through a terminal connected to the blade's serial interface.

The terminal can be connected to display VGA text information. Terminal keyboard input is redirected and treated as a normal PC keyboard input. The serial console redirection feature can be configured via a setup utility.

4.2.1 Requirements

For serial console redirection, the following is required:

- Terminal or terminal emulation which supports a VT100 or ANSI mode
- NULL-modem cable

Terminal emulation programs such as TeraTermPro can be used. In order to use TeraTermPro using the function keys, the keyboard configuration file of TeraTermPro has to be modified as follows:

Table 4-1 BIOS Key Codes for Terminal Emulation Program

Function Key	Key Code
PF1	59
PF2	60

4.2.2 Default Access Parameters

By default, the blade can be accessed using the serial interface COM1. This interface is using a RJ-45 connector at the blade's face plate.

A NULL-Modem cable is available as accessory kit for the blade. It converts the RJ-45 connector to a standard DSUB connector which can be connected to a remote terminal. The following communication parameters are used, by default:

- Baud rate: 9600
- Flow control: None
- VT-100
- 8 data bits
- No parity
- 1 stop bit

4.2.3 Connecting to the Blade

Procedure

In order to connect to the blade using the serial console redirect feature, proceed as follows:

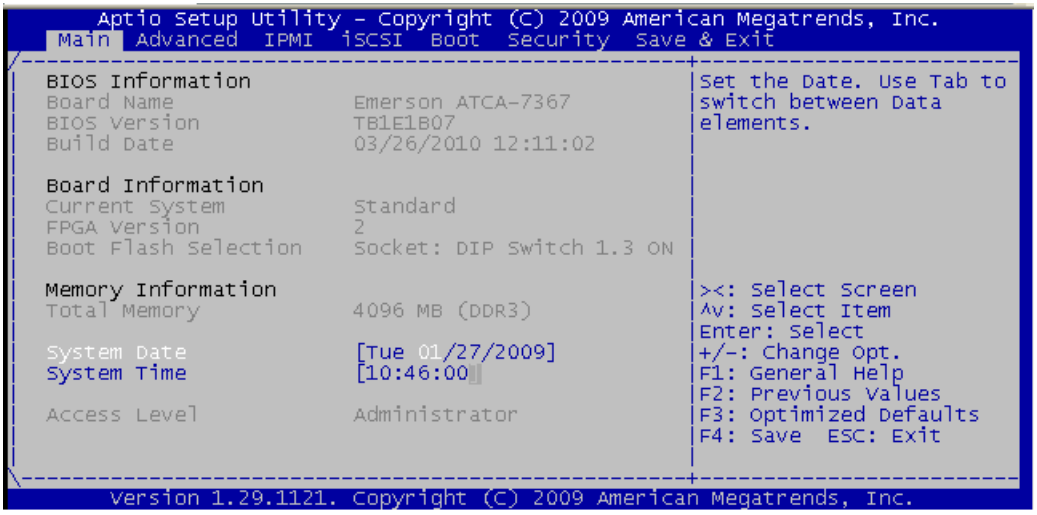
1. Configure terminal to communicate using the same parameters as in BIOS setup.
2. Connect terminal to NULL-modem cable.
3. Connect NULL-modem cable to COM port of the blade.
4. Start up blade.

4.3 Changing Configuration Settings

When the system is turned on or rebooted, the presence and functionality of the system components is tested by POST (Power-On Self-Test).

Press <F2> when requested. The main menu appears. It looks similar to the one shown in the following figure.

Figure 4-1 Main Menu



- Make sure that BIOS is properly configured prior to installing the operating system and its drivers.
- If you save changes in setup, the next time the blade boots BIOS will configure the system according to the setup selections stored. If those values cause the system boot to fail, reboot and enter setup to get the default values or to change the selections that caused the failure.

In order to navigate in setup, use the arrow keys on the keyboard to highlight items on the menu. All other navigation possibilities are shown at the bottom of the menu.

Additionally, an item-specific help is displayed on the right side of the menu window.

4.4 Boot Options

This section describes which boot devices are supported by the BIOS and how to select the boot device.

4.4.1 Supported Boot Devices

The BIOS supports booting from the following devices/sources:

- USB devices, such as floppy, CD ROM and hard disk
- Solid State Disk connected to the SATA interface. (available only when SSD SATA is assembled)
- Storage devices connected to the SAS controller (by RTM)
- Network (Front Panel Ethernet, Base Ethernet and Ethernet on RTM)
- Storage devices connected to the Fiber Channel module (via RTM)
- iSCSI block devices

4.4.2 Selecting The Boot Device

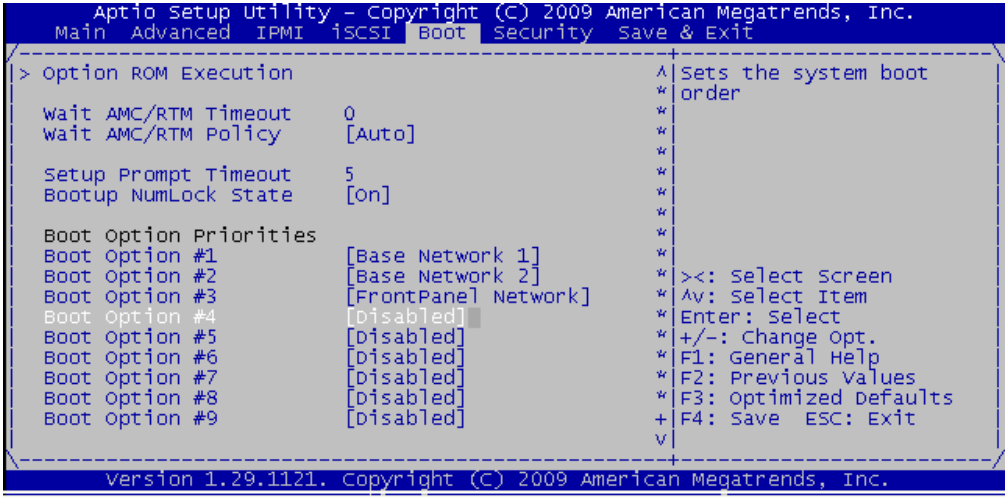
There are two possibilities to determine the device from which BIOS attempts to boot:

- By setup to select a permanent order of boot devices
- By boot selection menu to select any device for the next boot-up procedure only

By Setup

To select the boot device by setup, proceed as follows:

1. From the menu, select [Boot].



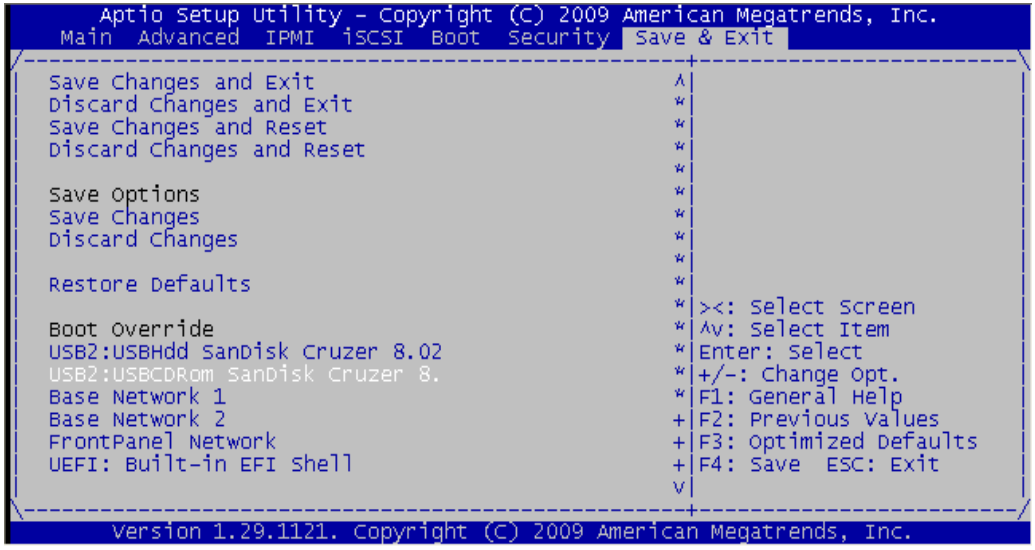
2. Select the order of the devices from which BIOS attempts to boot the operating system.
3. Enter the submenu "Option Rom Execution" to enable/disable booting from specific devices. Changes have to be saved and the board has to be rebooted when changing the Option Rom Execution.

If BIOS is not successful at booting from one device, it tries to boot from the next device on the list.

4.4.3 By Boot Selection Menu

1. From the menu, select [Save & Exit].
2. Override existing boot sequence by selecting another boot device from the boot override list.

Figure 4-2 Exit Menu



If the selected device does not load the operating system, BIOS resets the board and reverts to the previous boot sequence.

4.5 IPMI Boot Parameter

Many BIOS setup parameters and setup default parameters are stored as IPMI boot parameters within a non-volatile memory controlled by the IPMC. IPMI boot parameter supports USER and DEFAULT area. The USER area contains the current BIOS setup settings. The parameters in the USER area can be modified by the BIOS setup utility and can also be modified remotely by IPMI commands. For example, through shelf manager.

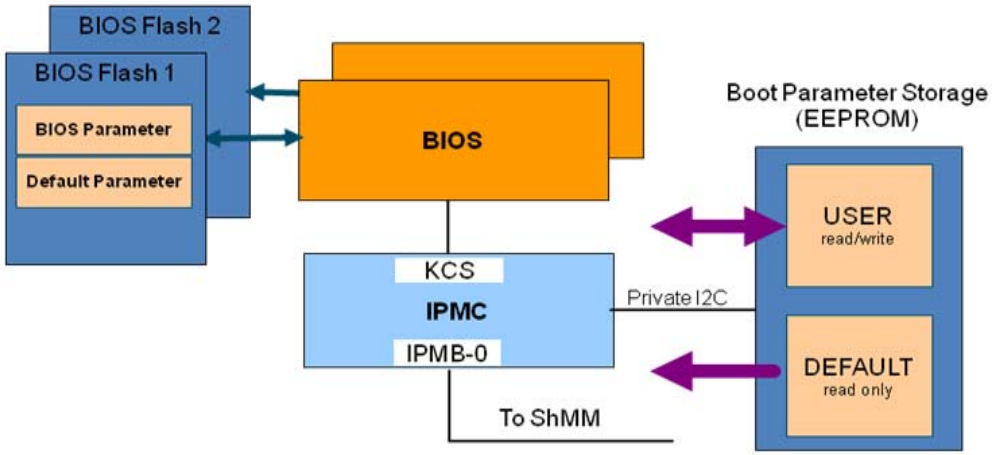
The DEFAULT area holds the BIOS default settings. This area is read only. BIOS default settings are loaded when selecting the Restore Defaults Item on BIOS Save & Exit Menu.

A detailed description of the IPMI Boot Parameter and the corresponding IPMI commands is available in the section *System Boot Options Parameter #100, on page 152*.

The main advantage of using IPMI boot parameter is that the parameters stored as IPMI boot parameters are not changed after a BIOS upgrade or a BIOS boot bank switch. BIOS will not return to the BIOS default settings after a BIOS upgrade.

Normally, the BIOS setup parameters are stored within the BIOS flash. The following figure and description helps you to understand how a BIOS setup parameter and an IPMI boot parameter interact.

Figure 4-3 IPMI Boot Parameter



Board Start

1. BIOS loads BIOS Parameter from Flash and uses them for initialization.
2. BIOS loads IPMI Boot Parameter from USER area.
3. BIOS updates the BIOS Parameter in the flash according to the IPMI Boot Parameter.
4. BIOS will reset the board if BIOS Parameter changes.

Change Settings

1. User enters the BIOS setup and changes some parameters.
2. User selects Save or Save and Exit option.
3. BIOS writes the parameter to the BIOS Parameter in the Flash.
4. BIOS writes the parameter to the IPMI Boot Parameter USER area.

Load Defaults

1. User enters BIOS setup and selects Load Defaults.
2. BIOS reads Default Parameter from Flash into the Setup.
3. BIOS reads IPMI Boot Parameter DEFAULT area into the Setup.
4. User select Save or Save and Exit option.
5. BIOS writes the parameter to the BIOS Parameter in the Flash.
6. BIOS writes the parameter to the IPMI Boot Parameter USER area.

4.6 Restoring BIOS Default Settings

The blade provides an on-board configuration switch that allows to load BIOS settings from the DEFAULT area of the IPMI Boot Parameters. In order to restore the BIOS default settings using this switch, you have to proceed as follows.

Procedure

To restore the BIOS default settings, proceed as follows:

1. Remove the blade from the system.
   See *Installing and Removing the Blade* on page 56 for the exact procedure.

2. Set the on-board switch SW4-3 OFF and SW4-4 ON.
   See *Switch Settings* on page 48 for the exact location of SW4.
3. Install and power up the blade.
   See *Installing and Removing the Blade* on page 56 for the exact procedure.
4. Wait until the blade has completely booted and is up and running.
5. Remove the blade from the system again.
   See *Installing and Removing the Blade* on page 56 for the exact procedure.
6. Set switch SW4-3 and SW4-4 to OFF.
   Now the BIOS default settings are restored.

4.7 Support for 116 Watt Slots

In order to run the board in a 116 watt slot, the ATCA-7367 IPMC offers two ATCA power levels: one with 116 watt and one with 152 watt. If the shelf manager selects the 116 watt power level, BIOS reduces the number of P-states (Performance states) for both CPUs in the ACPI table to meet the 116 watt power dissipation requirement for this slot. When the operating system has booted and the board runs in 152 watt mode the CPU frequency reaches up to 2.0 GHz. in 116 watt mode the highest CPU frequency is 1.73 GHz.

The selected ATCA power level is displayed on the console at power up and after reset:

```
ATCA Power Level 1: 116 Watt - P-States Limited
or
ATCA Power Level 2: 152 watt - No Power Limit
```

When the board is plugged into a 116 Watt slot, the board runs with reduced performance.

4.8 LED Usage

BIOS uses LEDs U1, U2 and U3 on the front panel to indicate activity of start up progress.

In boot loader phase (PEI phase) U1 and U2 glow red, U3 is glowing alternately red, green and orange.

In main initialization phase (DXE phase) only U3 is glowing alternately red, green and orange. U1 and U2 are set to the default value: base Ethernet interface link and activity LEDs. The individual colors of U3 do not have any meaning. U3 is just an indicator for boot progress.

Shortly before closing BIOS and starting an operating system, LED U3 is set to OFF.

4.9 Upgrading the BIOS

A BIOS upgrade kit for the blade is available. This allows the BIOS to be upgraded. The BIOS upgrade kit contains documentation which describes in detail how to upgrade the BIOS.

Update tool for Linux is provided with Basic Blade Services (BBS). For details on how to upgrade BIOS from Linux, please refer to *Basic Blade Services Software for the ATCA-7367 Programmer's Reference*.

After performing a BIOS upgrade or after restoring a corrupted BIOS image, all BIOS settings are reset to their default values except for parameters that are stored in IPMC storage area.

4.10 BIOS Error Messages

In some cases, the BIOS prints error messages to the console. For example, an error message is printed when the CMOS battery is bad or was removed. In case of memory errors, BIOS disables the defective DIMM module and prints a message similar to the one below and continues:

```
Memory Error Detected: Disable DIMM 0 Channel 1 Node 0 (DIMM Socket
P03)
ERROR: Minor (40) ComputingUnit (0) Memory (5): None Useful (100a)
```

In this example, the DIMM module in socket P03 is disabled.

When BIOS does not find useful memory, it prints the following message and stops.

```
FATAL ERROR: No Memory Found (E8/01)
ERROR: Major (80) ComputingUnit (0) Memory (5): None Detected (1009)
```

4.11 BIOS Setup Utility

The BIOS incorporates a setup utility that allows the user to alter a variety of system options. This section describes the operation of the utility by describing the various options available through a set of hierarchical menus. Not all options are available with all products and some depend on BIOS customizations.

The current settings are stored in the SPI FLASH NVRAM area and any changes can be copied back to this area via the Exit menu. The operation of the BIOS defaults is described later in this document.

To start the utility, you must press the F2 key during the early stages of POST after power-up. Note that this functionality operates with USB keyboards when enabled, and via the console redirection facility when enabled.

The table below briefly describes the primary menus, most of which have sub-menus. The following sections describe the menus in detail.

Table 4-2 Primary Menu Description

Menu	Options
Main	BIOS information, memory information and date and time
Advanced	WHEA, CPU, Runtime Error Logging, Chipset-North Bridge, Chipset-South Bridge, SATA, USB, SuperIO, Serial Port Console Redirection and Network Stack options.
IPMI	IPMI information, SEL and FRU options.
iSCSI	iSCSI Initiator Name options.
Boot	Option ROM Execution, Boot mode and Boot options.
Security	Administrator and User password options.
Save & Exit	Save with or without changes, Load/save default settings and Boot Device Override options.
Event Logs	View Smbios Event Logs and System Event Logs. This menu is not intended for Customer use. It is for internal debugging purpose only.

The Aptio navigation can be accomplished using a combination of the keys. These keys include the <FUNCTION> keys, <ENTER>, <ESC>, <ARROW> keys, and so on.

Table 4-3 Aptio Navigation

Key	Description
ENTER	The Enter key allows the user to select an option to edit its value or access a sub menu.
>< Left/Right	The Left and Right <Arrow> keys allow you to select a screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
^v Up/Down	The Up and Down <Arrow> keys allow you to select an item or sub-screen.
+- Plus/Minus	The Plus and Minus <Arrow> keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The <Tab> key allows you to select fields.
ESC	The <Esc> key allows you to discard any changes you have made and exit the Aptio Setup. When you are in sub-menu, <Esc> allows you to exit to the upper menu.
Function keys	When other function keys become available, they are displayed at the right of the screen along with their intended function.
F1	General Help
F2	Load Previous Values.
F3	Load Optimized Defaults.
F4	Save ESC & Exit

4.11.1 Main Menu

Figure 4-4 Main Menu

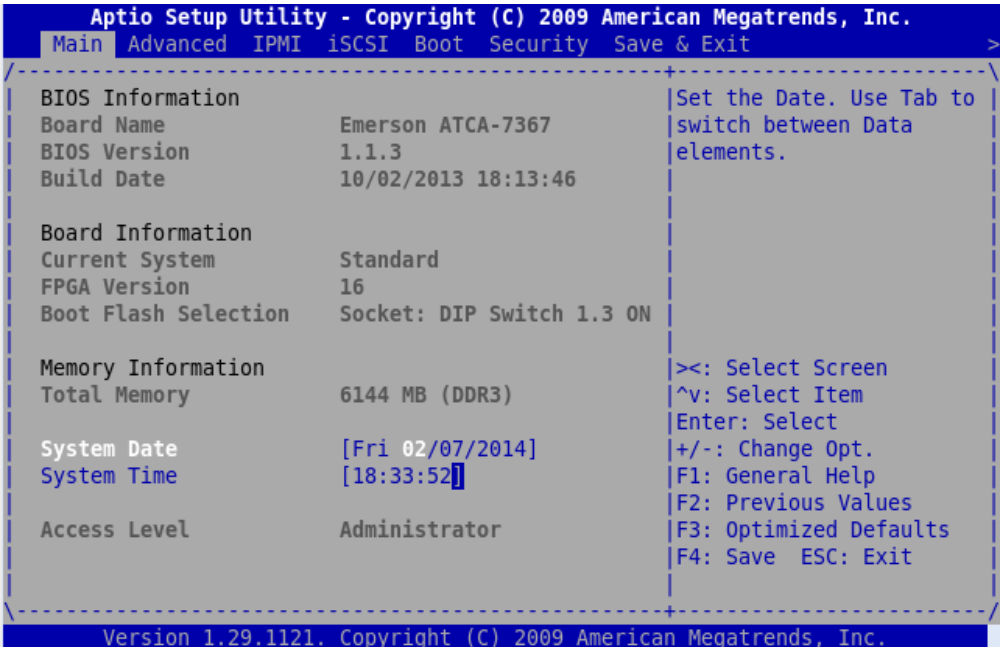


Table 4-4 Main Menu Description

Field	Description
BIOS Name	Artesyn board name.
BIOS Version	Artesyn BIOS version.
Build Date	BIOS build date.
Total Memory	Total memory fitted.
System Date	Sets the time and date (month/day/year format). To change these values, go to each field and enter the desired value. Press the tab key to move from hour to minute to second, or from month to day to year. There is no default value.
System Time	

4.11.2 Advanced Menu

Figure 4-5 Advanced Menu

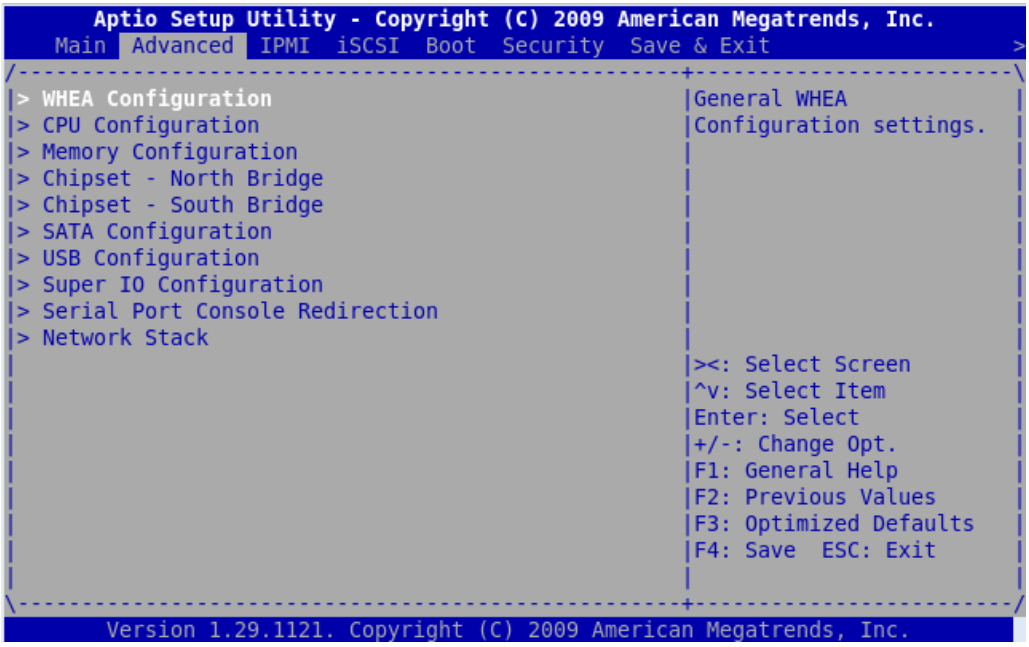


Table 4-5 Advanced Menu Description

Field	Description
WHEA Configuration	General WHEA Configuration settings. See later separate section for details.
CPU Configuration	CPU Configuration Parameters. See later separate section for details.
Chipset - North Bridge	North Bridge Parameters. See later separate section for details.
Chipset - South Bridge	South Bridge Parameters. See later separate section for details.
SATA Configuration	SATA Devices Configuration Parameters. See later separate section for details.
USB Configuration	USB Configuration Parameters. See later separate section for details.

Table 4-5 Advanced Menu Description (continued)

Field	Description
Super IO Configuration	System Super IO chip Parameters. See later separate section for details.
Serial Port Console Redirection	Serial Port Console Redirection Configuration Parameters. See later separate section for details.
Network Stack	Network stack settings. See later separate section for details.

4.11.2.1 WHEA Configuration

Table 4-6 WHEA Configuration

Field	Description
WHEA Support	Enable or disable Windows Hardware Error Architecture. Default is Enabled.

4.11.2.2 CPU Configuration

Table 4-7 CPU Configuration

Field	Description
Processor Type	Processor Type
EMT64	EMT64 support status
Processor Speed	Processor Speed
Processor Stepping	Processor Stepping
Microcode Revision	Microcode Revision
Processor Cores	Processor Cores number
Intel HT Technology	Intel HT Technology support status
Hyper-threading	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled. Default is Enabled.

Table 4-7 CPU Configuration (continued)

Field	Description
Active Processor Core	Number of cores to enable in each processor package. Options: ALL, 1, 2. Default is ALL.
Limit CPUID Maximum	Limit CPUID Maximum. Options: Disabled and Enabled. Disabled for Windows XP. Default is Disabled.
Hardware Prefetcher	To enable/disable the MLC streamer prefetcher. Options: Disabled and Enabled. Default is Enabled.
Adjacent Cache Line Prefetch	To enable/disable prefetching of adjacent cache lines. Options: Disabled and Enabled. Default is Enabled.
Intel Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. Options: Disabled and Enabled. Default is Enabled.
Turbo Mode	Enable/Disable Intel Turbo mode. Options: Disabled and Enabled. Default is Enabled.
Performance/Watt	Optimized - Turbo Boost engages after the highest performance state is sustained for more than two seconds. Traditional - Intel Turbo Boost Technology is engaged immediately when possible.

4.11.2.3 MemoryConfiguration

Table 4-8 Memory Configuration

Field	Description
DIMM Information	Submenu for displaying DIMM presence and size information.
QPI Link	QPI Link Speed and Frequency Configuration Page.
Total Memory	Total Memory fitted.
Current Memory Mode	Current Memory Mode.
Current Memory Speed	Current Memory Speed.
Mirroring	Mirroring support status.

Table 4-8 Memory Configuration

Field	Description
Sparing	Sparing support status.
DIMM Information	Display DIMM presence and Size information.
Memory Mode	Select the mode for memory initialization. Options: Independent, Mirroring and Lock Step. Default is Independent.
channel Interleaving	Select different Channel Interleaving setting. Options: Auto, 6 Way, 4 Way, 3 Way, 2 Way and 1 Way. Default is Auto.
Rank Interleaving	Select different rank Interleaving setting. Options: Auto, 4 Way, 3 Way, 2 Way and 1 Way. Default is Auto.
Hardware Memory Test	Disabling this option results in HW memory test being bypassed by MRC. Options: Disable and Enable. Default is Enable.

4.11.2.4 Chipset - North Bridge

Table 4-9 Chipset - North Bridge

Field	Description
Tylersburg IOH Configuration	Tylersburg IOH Configuration page. See later separate section for details.
Auto-Detect RTM	If enabled, the RTM is detected and the RTM PCIe parameter are set for this RTM. If disabled, the RTM PCIe parameter can be set manually.
RTM PCIe Gen1 Speed	This option force RTM PCIe root ports to Gen1 operation. If this option is disabled, RTM PCIe support both Gen1 and Gen2 devices. This option is active when Auto-Detect RTM is set to "Enable".
PCIe to RTM	Selects PCIe port Bifurcation for Zone 3 connector (RTM). This option is active when Auto-Detect RTM is set to "Enable".

4.11.2.4.1 Intel(R) VT for Directed I/O Configuration

Table 4-10 Intel(R) VT for Directed I/O Configuration

Field	Description
Intel(R) VT-d	Enable/Disable Intel(R) Virtualization Technology for Directed I/O. Options: Disabled and Enabled. Default is Disabled.
Interrupt Remapping	Enable/Disable VT-d Engine Interrupt Remapping support if Intel(R) VT-d is enabled. Options: Disabled and Enabled. Default is Enabled.
Coherency Support	Enable/Disable VT-d Engine Coherency support
ATS Support	Enable/Disable VT-d Engine Address Translation Services (ATS) support.
Pass-through DMA	Enable/Disable VT-d Engine Pass through DMA support.

4.11.2.4.2 IOH Thermal Sensors

Table 4-11 IOH Thermal Sensors

Field	Description
Thermal Sensors	Enable/Disable integrated North Bridge thermal sensors. Recommended value: Disable
Low Threshold	Low temperature threshold for thermal sensor.
High Threshold	High temperature threshold for thermal sensor.
Catastrophic Threshold	Critical temperature threshold for thermal sensor.

4.11.2.5 Chipset - South Bridge

Table 4-12 Chipset - South Bridge

Field	Description
GbE Controller	Enable/Disable GbE controller. Options: Disable and Enable. Default is Enable.
USB Configuration	USB Configuration Parameters page. See later separate section for details.
PCIE Root Ports Configuration	PCIE Root Ports Configuration

4.11.2.5.1 USB Configuration

Table 4-13 USB Configuration

Field	Description
All USB Devices	Enable/Disable All USB Devices ports. Options: Disabled and Enabled. Default is Enabled.
USB 2.0(EHCI) Support	Enable/Disable USB 2.0 (EHCI) Support. This option doesn't take effect if "All USB Devices" option is disabled. Options: Disabled and Enabled. Default is Enabled.
Front Panel USB	Enable/Disable Front Panel USB port 1. This option doesn't take effect if "All USB Devices" option is disabled. Options: Disabled and Enabled. Default is Enabled.
OnBoard USB FlashDisk	Enable/Disable OnBoard USB FlashDisk. This option doesn't take effect if "All USB Devices" option is disabled. Options: Disabled and Enabled. Default is Enabled.

Table 4-13 USB Configuration (continued)

Field	Description
ARTM USB	Enable/Disable RTM USB port. This option doesn't take effect if "All USB Devices" option is disabled. Options: Disabled and Enabled. Default is Enabled.

4.11.2.5.2 PCIE Root Ports Configuration

Table 4-14 PCIE Root Ports Configuration

Field	Description
PCIE Configuration	To be configured as x1 or x4 link

4.11.2.6 SATA Configuration

Table 4-15 SATA Configuration

Field	Description
SATA Port0 (Debug)	SATA device present status. Or disabled by below SATA Mode.
SATA Port1 (Zone 3)	SATA device present status. Or disabled by below SATA Mode.
SATA Port5 (AMC)	SATA device present status. Or disabled by below SATA Mode.
SATA Mode	Determines how SATA controllers operate. Options: Disable, IDE mode, AHCI mode and RAID mode. Default is IDE.
Serial-ATA Controller 0	Enable/Disable Serial-ATA Controller 0. This option is only valid when SATA Mode is IDE mode. Options: Disable, Enhanced and Compatible. Default is Compatible.
Serial-ATA Controller 1	Enable/Disable Serial-ATA Controller 1. This option is only valid when SATA Mode is IDE mode. Options: Disable and Enhanced. Default is Enhanced.

4.11.2.7 USB Configuration

Table 4-16 USB Configuration

Field	Description
USB Devices	List the USB Devices attached.
Legacy USB Support	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications. Options: Enabled, Disabled and Auto. Default is Enabled.
EHCI Hand-off	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver. Default is Enabled.
Port 60/64 Emulation	Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.
USB transfer time-out	The time-out value for Control, Bulk, and Interrupt transfers.
Device Reset Timeout	USB mass storage device Start Unit command timeout. Items: 10 sec,20 sec,30 sec,40 sec. Default is 20 sec.
Device Power-up delay	Maximum time the device will take before it properly reports itself to the Host Controller.
Mass Storage Devices	Mass Storage Devices list. For each Mass Storage Device, there is the following item to set emulation type.
Mass Storage Device Emulation Type	Mass storage device emulation type. 'AUTO' enumerates devices according to their media format. Optical drives are emulated as 'CDROM', drives with no media will be emulated according to a drive type. Options: Auto, Floppy, Forced FDD, Hard Disk and CD-ROM. Default is Auto.

4.11.2.8 Super IO Configuration

Table 4-17 Super IO Configuration

Field	Description
Super IO Chip	The Super IO device is fixed to FPGA Serial Devices.
Serial Port 0 Configuration	Set Parameters of Serial Port 0 (COMA). See later separate section for details.

4.11.2.8.1 Serial Port 0 Configuration

Table 4-18 Serial Port 0 Configuration

Field	Description
Serial Port	Enable/Disable Serial Port. Default is Enabled.
Change Settings	Select an optimal setting for Super IO Device. This option is only valid when Serial Port is enabled. Options: Auto IO=3F8h; IRQ=4 IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12 Default is IO=3F8h; IRQ=4

4.11.2.9 Serial Port Console Redirection

Table 4-19 Serial Port Console Redirection

Field	Description
COM0: Console Redirection	Enable/Disable Console Redirection. Default is Enabled.

Table 4-19 Serial Port Console Redirection (continued)

Field	Description
COM0: Console Redirection Settings	See later separate section for details.
Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS): Console Redirection	Enable/Disable Console Redirection. Default is Enabled.
Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS): Out-of-Band Mgmt Port	COM0
Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS): Data Bits	8
Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS): Parity	None
Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS): Stop Bits	1
Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS): Terminal Type	VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation. This option is only valid when EMS Console Redirection is enabled. Options: VT100, VT100+, VT-UTF8 and ANSI. Default is VT-UTF8.

4.11.2.9.1 COM0 Console Redirection Settings

Table 4-20 COM0 Console Redirection Settings

Field	Description
Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes. Options: VT100, VT100+, VT-UTF8 and ANSI. Default is VT100.
Bits per second	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds. Options: 9600,19200,57600 and 115200. Default is 9600.
Data Bits	Data Bits. Options: 7 and 8. Default is 8.
Parity	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Options: None, Even, Odd, Mark and Space. Default is None.
Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. Options: 1 and 2. Default is 1.
Resolution 100x31	Enables or disables extended terminal resolution.
Legacy OS Redirection	On Legacy OS, the number of Rows and Columns supports redirection
80x25 and 100x31. Default is 80x25.	

4.11.2.10 Network Stack

Table 4-21 Network Stack

Field	Description
Network stack	Enable/Disable the network stack(Pxe and UEFI). Options: Disable and Enable. Default is Disable.

4.11.3 IPMI Menu

Figure 4-6 IPMI Menu

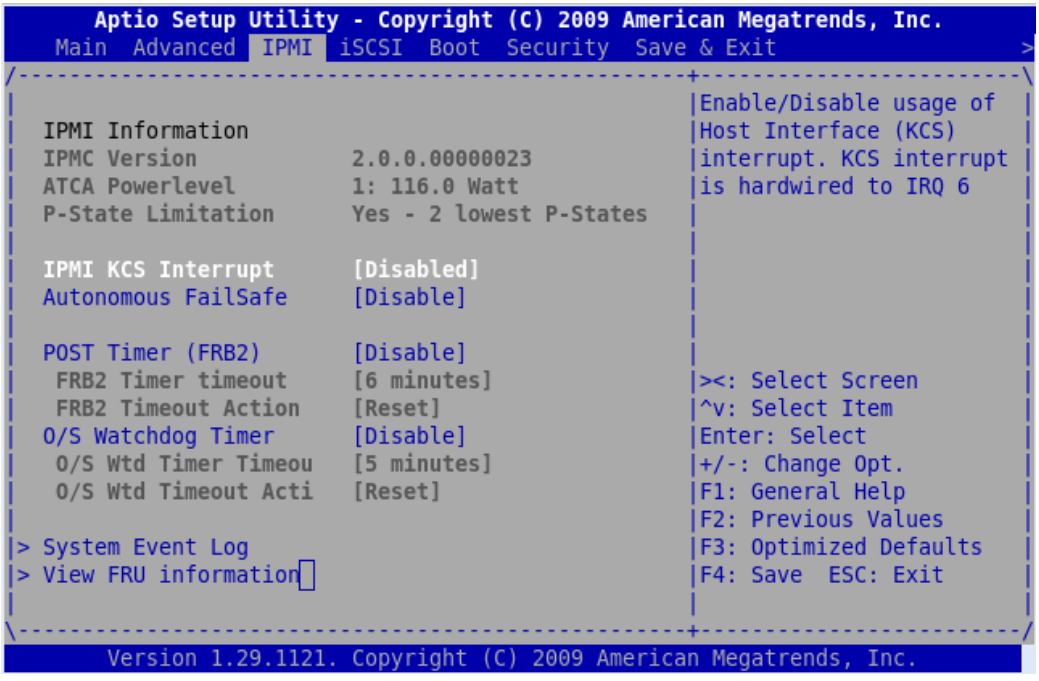


Table 4-22 IPMI Menu

Field	Description
IPMC Version	IPMC version.
ATCA Powerlevel	ATCA Powerlevel.
P-State Limitation	P-State Limitation
IPMI KCS Interrupt	Enable/Disable of Host Interface (KCS) Interrupt. KCS Interrupt is hardwired to IRQ 6.1
Autonomous FailSafe	If enabled, BIOS will switch to backup BIOS bank automatically if the BIOS image is corrupted or the IPMC watchdog (FRB2) is timed-out by the BIOS hang-up or other BIOS boot fails.
POST Timer (FRB2)	Enable or Disable FRB2 timer (POST timer). Options: Enable and Disable. Default is Disable.
FRB2 Timer Timeout	Enter value Between 3 to 6 min for FRB2 Timer Expiration value. This option is only valid when POST Timer (FRB2) is enabled. Options: 3 minutes, 4 minutes, 5 minutes and 6 minutes. Default is 6 minutes.
FRB2 Timer out Action	Configure how the system should respond if the Frb2 Timer expires. Not available if Frb2 Timer is disabled. Options: Do Nothing, Reset and Power Down. Default is Reset.
O/S Watchdog Timer	If enabled, starts a BIOS timer which can only be shut off by Intel Management Software after the OS loads. Helps to determine that the OS successfully loaded or follows the O/S Boot Watchdog Timer policy.
O/S wtd: Timer Timeout	Configure the length of the O/S Boot Watchdog Timer. Not available if O/S Boot Watchdog Timer is disabled. Options: 5 minutes, 10 minutes, 15 minutes and 20 minutes. Default is 10 minutes.
O/S wtd Timerout Action: Timer Policy	Configure how the system should respond if the O/S Boot Watchdog Timer expires. Not available if O/S Boot Watchdog Timer is disabled. Options: Do Nothing, Reset and Power Down. Default is Reset.
System Event Log	Sel Event Log configuration page. See later separate section for details.
View FRU information	FRU information page. See later separate section for details.

4.11.3.1 System Event Log

Table 4-23 System Event Log

Field	Description
Log EFI Status Codes	Disable the logging of EFI Status Codes or log only error code or only progress code or both. Options: Disabled, Both, Error code and Progress code. Default is Both. NOTE: All values changed here do not take effect until computer is restarted.

4.11.3.2 View FRU Information

Table 4-24 View FRU Information

Field	Description
System Manufacturer	Value should be gotten from IPMC FRU.
System Product Name	Value should be gotten from IPMC FRU.
System Version	Value should be gotten from IPMC FRU.
System Serial Number	Value should be gotten from IPMC FRU.
Board Manufacturer	Value should be gotten from IPMC FRU.
Board Product Name	Value should be gotten from IPMC FRU.
Board Version	Value should be gotten from IPMC FRU.
Board Serial Number	Value should be gotten from IPMC FRU.
Chassis Manufacturer	Value should be gotten from IPMC FRU.
Chassis Product Name	Value should be gotten from IPMC FRU.
Chassis Serial Number	Value should be gotten from IPMC FRU.
SDR Revision	Value should be gotten from IPMC FRU.

4.11.4 iSCSI Menu

Figure 4-7 iSCSI Menu

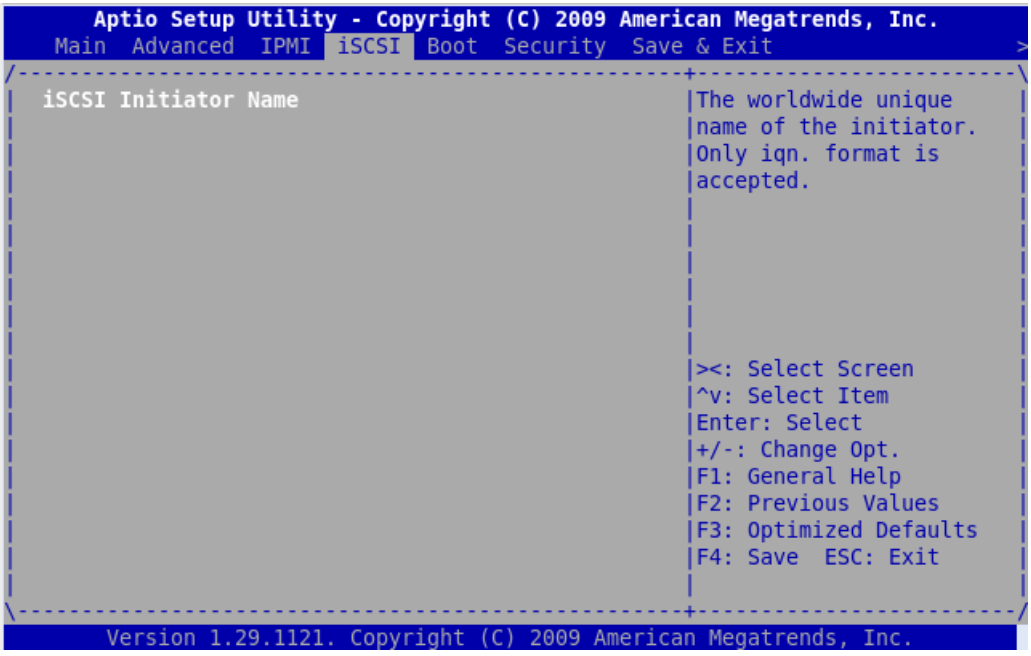


Table 4-25 iSCSI Menu Description

Field	Description
iSCSI Initiator Name	The worldwide unique name of the initiator. Only iqn. format is accepted.
Port xx-xx-xx-xx-xx-xx	Set the iSCSI parameters on port xx-xx-xx-xx-xx-xx page. The options are only visible when Network Stack is enabled. Xx-xx-xx-xx-xx-xx is the iSCSI port MAC address. See later separate section for details.

4.11.4.1 iSCSI Port xx-xx-xx-xx-xx-xx

Table 4-26 iSCSI Port xx-xx-xx-xx-xx-xx

Field	Description
Enable iSCSI	Enable/Disable iSCSI feature on the port. Options: Disabled and Enabled. Default is Disabled.
Enable DHCP	Enable/Disable DHCP on the port. Options: Disabled and Enabled. Default is Disabled.
Get target info via DHCP	Get target info via DHCP. This option is only valid when DHCP is enabled. Options: Disabled and Enabled. Default is Disabled.
Initiator IP Address	Enter Initiator IP address in dotted-decimal notation. This option is only valid when DHCP is disabled. Default is 0.0.0.0
Initiator Subnet Mask	Enter Initiator subnet mask in dotted-decimal notation. This option is only valid when DHCP is disabled. Default is 0.0.0.0
Gateway	Enter Initiator gateway IP address in dotted-decimal notation. This option is only valid when DHCP is disabled. Default is 0.0.0.0
Target Name	Enter iSCSI Target Name. This option is only valid when DHCP is disabled or when DHCP is enabled and 'Get target info via DHCP' is disabled.
Target IP Address	Enter Target IP address in dotted-decimal notation. This option is only valid when DHCP is disabled or when DHCP is enabled and 'Get target info via DHCP' is disabled. Default is 0.0.0.0
Target Port	Enter Target port number. This option is only valid when DHCP is disabled or when DHCP is enabled and 'Get target info via DHCP' is disabled. Default is 3260.
Boot LUN	Enter Target LUN number. This option is only valid when DHCP is disabled or when DHCP is enabled and 'Get target info via DHCP' is disabled. Default is 0.
CHAP Type	CHAP Type. Options: None, One way and Mutual. Default is None.
Save Changes	Save changes.
Back to Previous Page	Go back to Previous Page.

4.11.5 Boot Menu

Figure 4-8 Boot Menu

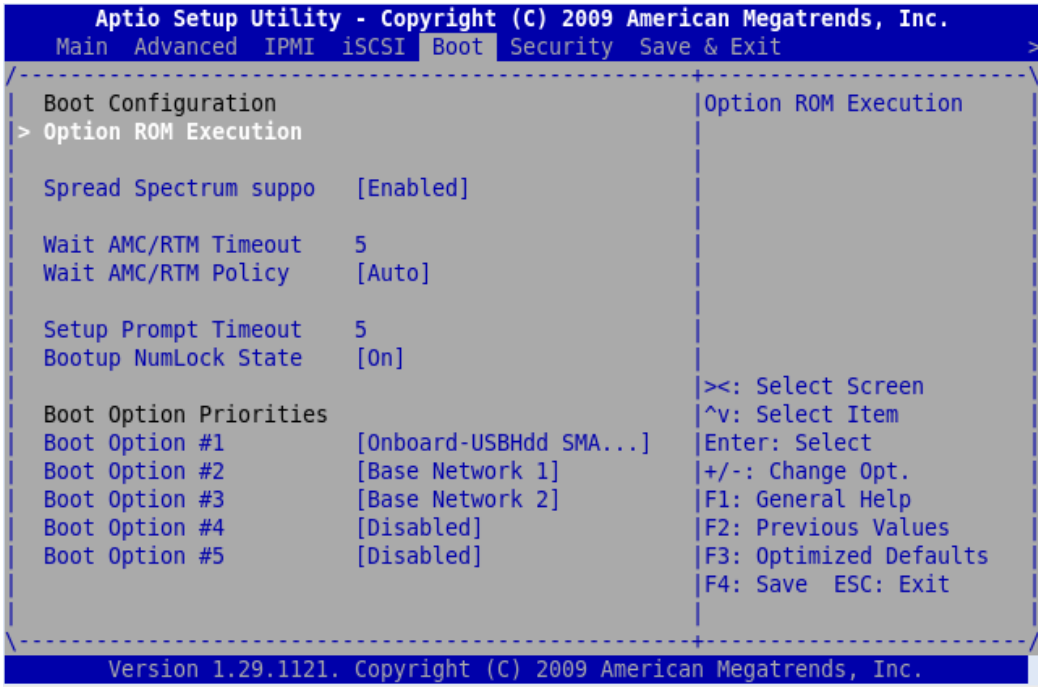


Table 4-27 Boot Menu

Field	Description
Option ROM Execution	Option ROM Execution Configuration page. See later separate section for details.
Spread Spectrum support	Enable Spread Spectrum
Wati AMC/RTM Timeout	Number of seconds before starting PCI devices init. Range 0-255
Wait AMC/RTM Policy	Force: The BIOS waits specified seconds before starting PCI devices init. Auto: The BIOS detects AMC/RTM automatically and continues to initialize PCI devices before the time expires.

Table 4-27 Boot Menu (continued)

Field	Description
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting. 0 means no wait(not recommended). Press Enter to confirm the change. Default is 2.
Bootup NumLock State	Select the keyboard NumLock state. Options: On and Off. Default is On.
Boot Option #1	Boot device option #1.
Boot Option #2	Boot device option #2.
Boot Option #N	Boot device option #N.

4.11.5.1 Option ROM Execution

Table 4-28 Option ROM Execution

Field	Description
Front Panel Net Boot	Controls execution of the Option ROM for the Front Panel Ethernet controller. Options: Disabled and Enabled. Default is Enabled.
Base Network Boot	Controls execution of the Option ROM for the Base Interface Ethernet. Options: Disabled and Enabled. Default is Enabled.
ARTM Network Boot	Controls execution of the Option ROM for the Ethernet on the ARTM. Options: Disabled and Enabled. Default is Disabled.
ARTM SAS Boot	Controls execution of the Option ROM for the SAS controller on the ARTM. Options: Disabled and Enabled. Default is Enabled.

4.11.6 Security Menu

Figure 4-9 Security Menu

Table 4-29 Security Menu Description

Field	Description
Setup Administrator Password	Set Setup Administrator Password.
User Password	Set Setup User Password.

4.11.7 Save & Exit Menu

Figure 4-10 Save & Exit Menu

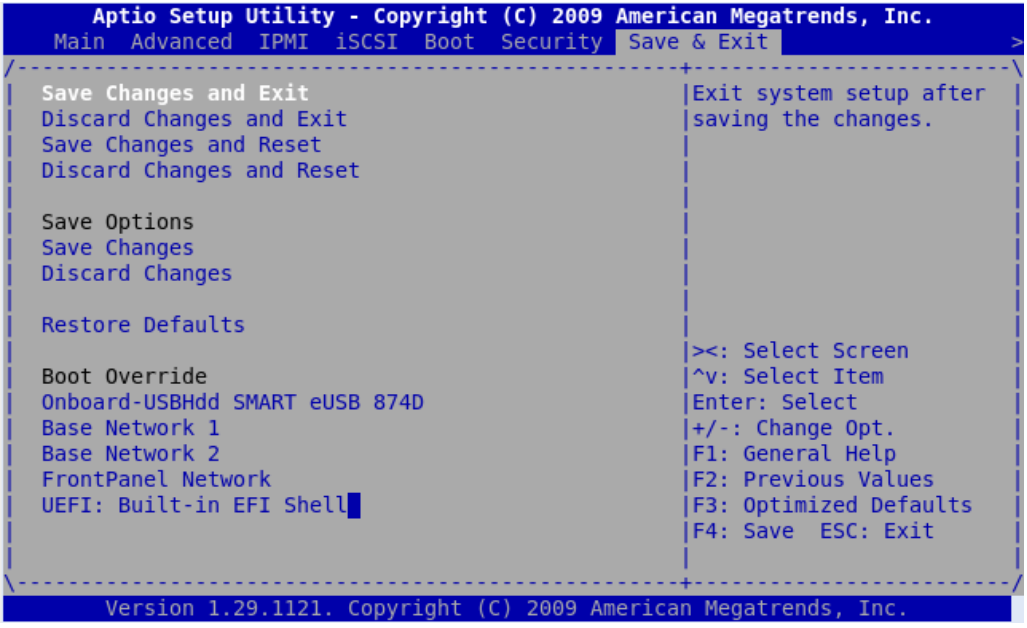


Table 4-30 Save & Exit Menu Description

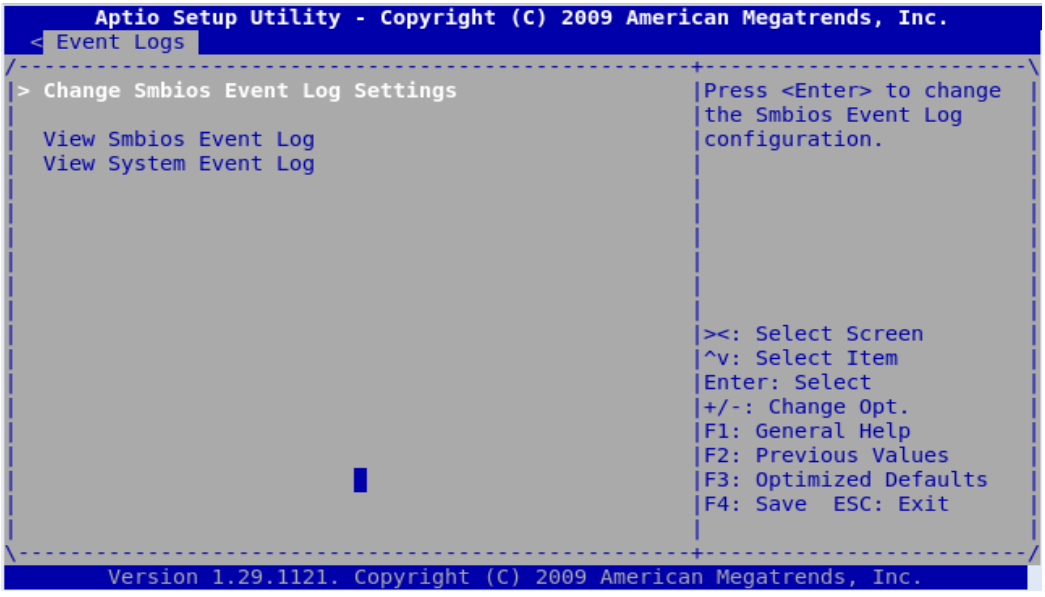
Field	Description
Save Changes and Exit	Exit system setup after saving the changes.
Discard Changes and Exit	Exit system setup without saving any changes.
Save Changes and Reset	Reset the system after saving the changes.
Discard Changes and Reset	Reset system setup without saving any changes.
Save Changes	Save Changes done so far to any of the setup options.
Discard Changes	Discard Changes done so far to any of the setup options.

Table 4-30 Save & Exit Menu Description (continued)

Field	Description
Restore Defaults	Restore/Load Defaults values for all the setup options. This option is the same as pressing F3.
Save as User Defaults	Save the changes done so far as User Defaults.
Restore User Defaults	Restore the User Defaults to all the setup options.
Boot Override	The options will override the boot orders in 'Boot' menu. So you can freely select the device which you want to boot to.

4.11.8 Event Logs Menu

Figure 4-11 Event Logs Menu



NOTICE

This menu is not intended for Customer use. It is for internal debugging purpose only.

Table 4-31 Event Logs Menu Description

Field	Description
Smbios Event Log	Change this to enable or disable all features of Smbios Event Logging during boot. Options: Enabled (Default), Disabled
Erase Event Log	Choose options for Choose options for Log. Erasing is done Log. Erasing is done activation during reset. Options: No (Default), Yes Next reset, Yes Every reset
When Log is Full	Choose options for reactions to a full Smbios Event Log Options: Do Nothing (Default), Erase Immediately
MECI	Multiple Event Count Increment: The number of occurrences of a duplicate event that must pass before the multiple-event counter associated with the log entry is updated, specified as a numeric value. Options: 1 (Default)
METW	Multiple Event Time Window: The number of minutes which must pass between duplicate log entries which utilize a multiple-event counter. The value ranges from 0 to 99 minutes. Options: 60 (Default)
Log OEM Codes	Enable or disable the logging of EFI Status Codes as OEM Codes (if not already converted to legacy). Options: Enabled (Default), Disabled
Convert OEM Codes	Enable or disable the logging of EFI Status Codes as OEM Codes (if not already converted to legacy). Options: Disabled (Default), Enabled
View Smbios Event Log	View SMBIOS Event Log
View System Event Log	View local System Event Log

4.12 BIOS Status Codes

The following table lists the BIOS status codes applicable to the used AMI UEFI BIOS. The BIOS status codes are stored in the blade's Port 80 register and can also be obtained by reading an on-board IPMI sensor.

4.12.1 Status Code Ranges

Table 4-32 Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC Status Codes & Errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution up to BDS
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xE8 - 0xEF	Memory initialization errors
0xB0 - 0xBF	Additional Memory Initialization Status Codes
0xE8 - 0xEE	Additional Memory Error Status Codes

4.12.2 Standard Status Codes

Table 4-33 SEC Status Codes

Status Code	Description
0x0	Not used

Table 4-33 SEC Status Codes (continued)

Status Code	Description
Progress Codes	
0x1	Power on. Reset type detection (soft/hard).
0x2	AP initialization before microcode loading
0x3	North Bridge initialization before microcode loading
0x4	South Bridge initialization before microcode loading
0x5	OEM initialization before microcode loading
0x6	Microcode loading
0x7	AP initialization after microcode loading
0x8	North Bridge initialization after microcode loading
0x9	South Bridge initialization after microcode loading
0xA	OEM initialization after microcode loading
0xB	Cache initialization
SEC Error Codes	
0xC – 0xD	Reserved for future AMI SEC error codes
0xE	Microcode not found
0xF	Microcode not loaded

Table 4-34 PEI Status Codes

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x15	Pre-memory North Bridge initialization is started
0x19	Pre-memory South Bridge initialization is started
0x2F	Memory initialization (other)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization

Table 4-34 PEI Status Codes (continued)

Status Code	Description
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization)
0x37	Post-Memory North Bridge initialization is started
0x3B	Post-Memory South Bridge initialization is started
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
Memory Initialization Codes	
0xB0	Chipset initialization
0xB1	Detect reset state
0xB2	DIMM detect
0xB3	Clock initialization
0xB4	Read SPD data
0xB5	early memory controller initialization
0xB6	Check DIMM population
0xB7	Channel initialization
0xB8	Channel training
0xB9	Run Build In Self Test
0xBA	Initialize memory map
0xBB	Setup RAS configuration
0xBF	Memory initialization complete
PEI Error Codes	
0x53	Memory initialization error. No usable memory detected
0x55	Memory not installed
0x56	Invalid CPU type or Speed

Table 4-34 PEI Status Codes (continued)

Status Code	Description
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	Reset PPI is not available
Memory Error Codes	
0xE8	No Memory
0xEA	DDR initialization error
0xEB	Memory test error
0xED	Mixed memory types
0xEE	Population error
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

Table 4-35 DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x78	ACPI module initialization
0x79	CSM initialization
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0xA0	IDE initialization is started

Table 4-35 DXE Status Codes (continued)

Status Code	Description
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAB	Setup Input Wait
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources

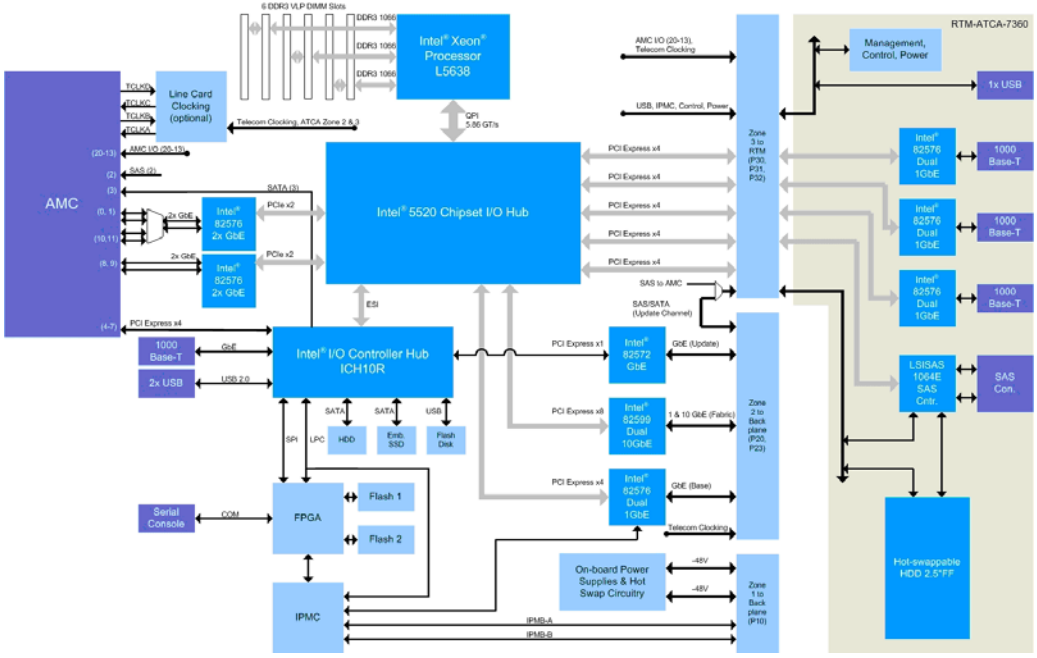
Table 4-35 DXE Status Codes (continued)

Status Code	Description
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

5.1 Block Diagram

The block diagram shows how the devices work together and the data paths used.

Figure 5-1 Block Diagram



5.2 Processor

Westmere-EP processor is a six-core processor, based on a 32 nm process technology first implementation of the Intel Nehalem ™ Micro architecture. The processor family features a range of thermal design power (TDP) envelopes from 40 W TDP up to 130 W TDP. The processor features two Intel QuickPath Interconnect point-to-point links capable of up to 6.4GT/S, 12MB of shared Last Level cache (L3), and an Integrated Memory Controller (IMC). The processor support all the existing Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3) and Streaming SIMD Extensions 4 (SSE4). The processor support several Advanced Technologies: Execute Disable Bit, Intel 64 Technology, Enhanced Intel SpeedStep Technology, Intel Virtualization Technology, and Simultaneous Multi Threading (SMT).

The following lists the main features of Westmere-EP processor:

- Socket: LGA 1366
- Core Speed: 2.0 GHz
- Cache Size
  - Instruction cache: 32Kb, per core
  - Data Cache: 32KB, per core
  - 256KB Mid-Level Cache (L2) per core
  - 12MB shared (L3) cache, running at core speed
- Data transfer rate: Two full-width Intel QuickPath Interconnect links, 5.86GT/s in each direction
- Multi-core support: up to six core per processor
- Integrated memory controller, supporting DDR3 Memory speed, 800, 1066, 1333MHz
- Package: 1366 balls, FC-BGA
- TDP: 40 W-130 W, varies depending on SKU.

The maximum power consumption of the processor allowed for ATCA-7367's NEBS application is 60 W.

5.3 Memory

The Westmere-EP has an integrated DDR3 Memory Controller supporting three independent channels of DDR3 memory. On ATCA-7367 each memory channel has two DIMM slots for a total of six DIMM slots. Below are the features of the IMC:

- Single-rank, dual-rank, six-rank DIMMs supported
- Registered and unbuffered DIMMs with or without ECC supported
- DDR3 speeds of 800,1066 and 1333 supported
- 512MB, 1GB, 2GB, 4GB chip technology supported

- RAS features supported with ECC DIMM (mirroring, x8/x4 SDDC, sparing, scrubbing)
- Memory error signaling for uncorrectable errors (Machine Check Exception (MCE) is signaled to all processors. CATERR# assertion can be used optionally to trigger SMI event.
- Memory error signaling for corrected memory errors by two independent mechanisms:
  - CMCI signaling based on Machine Check architecture.
  - SMI/NMI signaling based on CSR registers in the IMC.

On ATCA-7367, up to six VLP DIMMs are used, and VLP DIMM is available in Registered (RDIMM) version only.

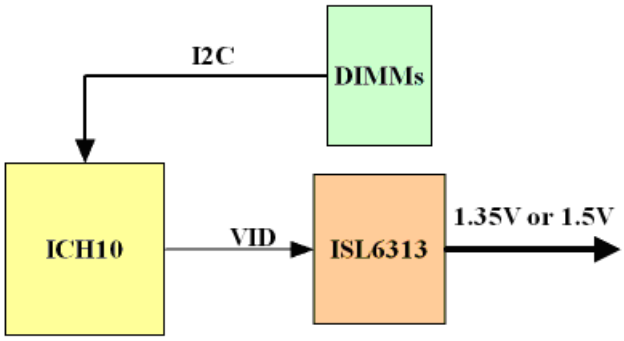
The following table shows the address of DIMM SPD in ATCA-7367 design.

Table 5-1 SPD I2C Address of DIMMs

DIMM	Address
DIMM1	0xA0
DIMM2	0xA2
DIMM3	0xA4
DIMM4	0xA6
DIMM5	0xA8
DIMM6	0xAA

ATCA-7367 supports 1.35 V and 1.5 V DDR3 technology. DDR3 power supply is controlled by VID code. BIOS will set up this VID to obtain the needed supply voltage according to DIMM SPD information, which is shown in the following figure:

Figure 5-2 1.35/1.5 V Voltage Selection for DIMMs



5.3.1 DDR3 Main Memory

ATCA-7367 provides a single Westmere-EP CPU with Integrated Memory Controller (IMC). IMC supports three independent 72-bit (64-bit Data + 8-bit ECC) wide DDR3 memory channels.

ATCA-7367 supports two VLP DIMM sockets for each memory channel resulting in a total of six DDR3 DIMM sockets.

Supported DDR3 speeds are DDR3-800 (PC3-6400), DDR3-1066 (PC3-8500), and DDR3-1333 (PC3-10600).

5.4 Chipset

The Intel 5520 chipset provides access to the I/O subsystem. The chipset provides up to 36 PCI Express generation 2 lanes. The blade makes use of 5 times x4 PCIe lanes routed to the Zone 3 connector.

The chipset is connected to the ICH10R I/O Controller via the Enterprise South Bridge Interface (ESI).

5.5 I/O Controller

The ICH10R provides extensive I/O interface support and the boot path to SPI Boot Flash devices for the processor. ICH10R is connected to the system through the Enterprise Southbridge Interface (ESI) of the Xeon 5520 chipset.

The following is a list of the main internal features and the I/O interface functions provided by the ICH10R Southbridge.

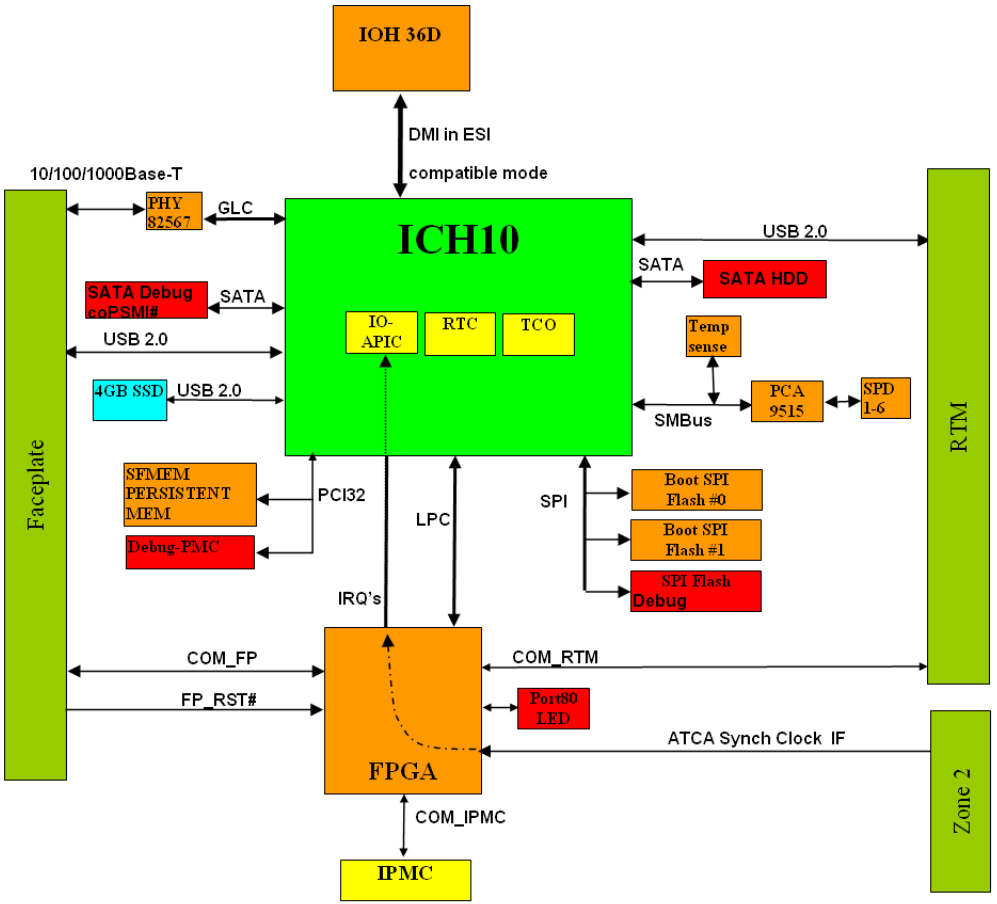
- Six x4 PCI Express 1.1 interface
- LPC interface
- SPI interface (Boot Flash): up to two devices 20 + 33 MHz
- Six serial ATA (SATA) interfaces (two used on ATCA-7367)
- Twelve USB 2.0 interfaces (four used on ATCA-7367)
- Two 8259 interrupt controllers and I/O APIC controllers
- Integrated I/O APIC
- Power management support
- Two 8237 DMA controller
- 8254-based Counter Timer/timers
- High-precision Event timers (HPET)
- RTC with 256-byte battery-backed SRAM
- System TCO (total cost of ownership) reduction circuits
- SMBus interface
- Two stage Watchdog timer

- PCI 2.3 interface 32-bit/ 33 MHz (connects to PMEM module)
- General purpose I/O pins

ATCA-7367 does not provide a legacy Super-I/O device and no legacy keyboard/mouse interface. Keyboard and mouse are supported through USB. Serial COM interfaces are provided from FPGA.

The following figure shows the I/O functions provided by ICH10R and those used on ATCA-7367:

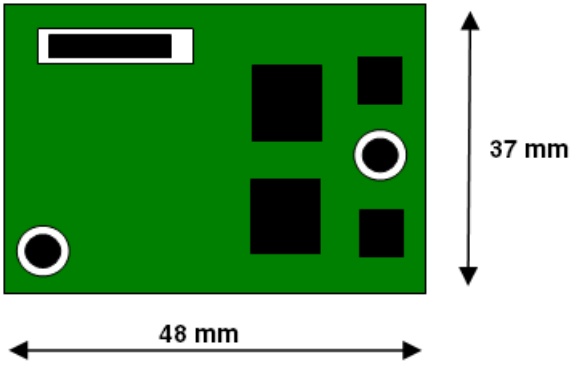
Figure 5-3 ICH10R Diagram



5.6 Persistent Memory Module (PMEM)

The ATCA-7367 provides a connector to assemble the Artesyn 7221-SFMEM (P/N #122265) module, a 48x37 low profile module integrating a PLX9030 PCI target-only Bridge and 64 Mb of Flash and 16 Mb of SRAM. The module connector is a 80-pin low density, low profile Molex Connector and features four configuration signals connected to the Glue Logic FPGA. Host and IPMC can configure the memory module through the configuration pins to use the FLASH as two 32 Mb mirrored banks (switchable, only one visible) or as continuous 64 MB Flash bank. Additionally, each bank is write protect able.

Figure 5-4 SFMEM-7221 Module dimensions (bottom view)



5.7 Ethernet Ports

The blade utilizes various Ethernet controllers that serve the ATCA Base I/F, Fabric I/F, Update Channel and Ethernet console. All Ethernet interfaces have 1GbE capability except for the Fabric I/F controller which can operate at 10 GbE or 1 GbE (PICMG 3.1 Option 9 and 1). The fabric I/F is fully operable in both 10G and 1G mode without the presence of an RTM.

One Ethernet port is available on the front panel. Additional Ethernet ports for external access are provided via the RTM.

The Ethernet controllers support I/O virtualization.

Table 5-2 Ethernet Controller Types

Interface	Location	Controller	Count	Ethernet Type
Base Interface	P23	Intel 82576	2 x	10,100,1G copper
Fabric Interface	P23	Intel 82599	2 x	10G/1G Serdes
Faceplate Interface	P27	Intel 82567	1 x	10,100,1 G Copper
Update Channel IF	P20	Intel 82572	1 x	1 G Serdes
AMC Interface	P500	2x Intel 82576	4 x	1 G Serdes

5.8 Storage

ATCA-7367 supports the following types of storage:

- Onboard HDD/SSD with standard 2.5 inch form factor
- Onboard SATA Cube
- Persistent RAM module
- Onboard USB Flash (eUSB)
- Storage RTM with SATA/SAS support
- Storage AMC

5.9 Storage Controller

Using an optional RTM, the blade provides a Serial Attached SCSI (SAS) controller. One on-board hard disk drive located on the RTM is connected to the controller. A minimum of two (2) ports are available on the RTM face plate. They can be used to attach an external storage RAID (JBOD). Another SAS port of the controller is routed to ATCA Zone 3 for the purposes of synchronizing with a RTM-based disk located in a logically paired ATCA slot.

5.10 Embedded Flash Disk

By default, the ATCA-7367 provides an onboard USB Flash module (4 GB) solid state disk. The disk can keep data, application SW and OS boot images. Booting from the device is supported. The flash disk controller provides a wear leveling algorithm to improve the longevity of the flash device.

5.10.1 SATA Embedded Flash Solid State Disc (SSD)

As an option, a SATA embedded flash SSD solution can be provided through assembly of the ATCA-7367/SATA module which is available as an accessory kit.

5.11 BIOS

ATCA-7367 provides a BIOS firmware that is stored in flash memory. It can be updated remotely via Ethernet or locally via operating system. Along with the BIOS and BIOS Setup program, the flash memory contains POST and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code.

A BIOS extension is provided for the RTM-based SAS controller to support RAID configuration.

5.12 IPMC

The blade features an Intelligent Platform Management Controller (IPMC) compliant to PICMG 3.0 and IPMI 1.5 and 2.0 (SOL only). The IPMC is a management subsystem providing monitoring, event logging, and recovery control. The IPMC serves as the gateway for management applications to access the payload hardware.

The IPMC firmware (FW) is stored in two independent memory images. Crisis recovery control is provided to allow reboot of the IPMC from a second image if the upgraded FW image is corrupted. FW images can be upgraded via HPM.1/IPMI using either IPMB or KCS interface.

The IPMC supports the initiation of a graceful shutdown of the host CPU. The IPMC can force the CPU to reset. It also controls the power and reset of the payload.

The IPMC provides a watchdog that supervises the payload. If enabled, the payload software needs to retrigger the Watchdog to prevent time-out. A watchdog time-out can generate a NMI, a payload reset or disabling/cycling of the payload power. The watchdog settings, including enable/disable, can be changed by payload software (setup menu). Time-out values can be selected from as short as seconds to as long as minutes.

The IPMC is supervised by a separate hardware Watchdog, which can not be disabled. IPMC FW retriggers the Watchdog timer.

The IPMC monitors the Port 80 POST codes generated by the payload CPU. The IPMC is connected to various sensors on the Blade that provide temperature sensor readings at all major devices and voltage sensor readings of all major voltages. The IPMC monitors reset events caused by devices like Watchdog, IPMI command, and reset button.

The FRU information of the various modules including front board, RTM, and other modules can be read via the IPMC and if necessary upgraded through the IPMC.

The IPMC features Serial over LAN (SOL) for the payload CPU serial console. The SOL interface is available via the ATCA Base I/F. SOL is activated by specific IPMI commands.

5.13 Serial Redirection

The CPU serial redirection reroutes the console input and output; that is the text output to the text screen and input from the standard keyboard. Typically, the console is used by the BIOS setup menus, BIOS initialization and boot routines, OS boot loaders and loaded OSs.

The serial console of the payload CPU is available via SOL. In addition to the SOL capability, the serial console is also available on the blade face plate using a RJ45 connector with Cisco pin-out. If a SOL session is established, only the output is available on the face plate. Input is not possible during this time via the face plate. Alternatively to the CPU serial console, the IPMC serial console is also available on the face plate serial connector. It can be selected via specific IPMI OEM command.

5.14 Serial Over LAN

Serial Over LAN (SOL) enables suitably designed blades and servers to transparently redirect a serial character stream of a baseboard UART to/from a remote client via LAN over RMCP+ sessions. This enables users at remote consoles to access the serial port of a blade/server and interact with a text-based BIOS console, operating system, command line interfaces, and serial text-based applications.

The IPMC provides a dedicated sideband connection (SMBus) to the Base Interface Ethernet controller. Data from the payload serial redirection is routed thru the sideband connection to the Base I/F. Vice versa, the Ethernet controller filters packets based on either MAC address, RMCP port number, or IP address and forwards them to the serial redirection over the sideband interface.

Client software like openIPMI is required to enable SOL and to communicate with the SOL based serial console.

5.15 USB 2.0 Interface

The ICH10R provides internal USB1.1/ USB 2.0 host controllers with up to twelve USB 2.0 ports. Two ports are routed to the faceplate, one port is used onboard to connect a USB 2.0 SSD User Flash Module and one port is routed to the RTM. The ports available at the faceplate are routed to a dual stacked connector. The ports are USB 2.0 compliant.

5.16 SMBus Interface

The SMBus interface of the ICH10R is connected to on-board devices like Clock PLL's, temperature sensors and the SPD PROMs of all twelve DDR3 DIMM memory modules. I^2C Bus Repeater of type PCA9515 is used to buffer the SMBus portion going to the SPD PROMs on the DIMM. The BIOS reads memory configuration parameters from SPD PROM. To address more than 8 memory I2C devices, the SMBus to the SPD PROMS is segmented.

Table 5-3 SMBus Devices

Device Name	Device Type	Address
SPD EEPROM	24C02	1010.000x b=A0
SPD EEPROM	24C02	1010.001x b=A2
SPD EEPROM	24C02	1010.010x b=A4
SPD EEPROM	24C02	1010.011x b=A6
SPD EEPROM	24C02	1010.100x b=A8
SPD EEPROM	24C02	1010.101x b=AA
Temp Sens#0	LM75	0x90
Temp Sens#1	LM75	0x92
DDR3 VREF_D margening	ISL90728	0x7C
Clock	ICS932S421	0xD2 + 0xD3
DB1200 clock	ICS9DB1200	0xDC + 0xDD
ICH10R Slave SMBus IF	ICH10R	0x88 + 0x89
Xeon 5520 (Tylersburg IOH36 D) Slave SMBus IF	Xeon 5520 (Tylersburg IOH36 D)	0xE0 (IOH Boostrap SMBUSID option is 0xC0)
MAX6618 PECI Hub	MAX6618	0x54

5.17 Real Time Clock

An external 32.768 kHz crystal sources the internal real time clock inside ICH10R with a frequency tolerance of 20 PPM. The RTC is fully-compliant with DS1287, MC14618, PC87911 and Y2K and provides 256 bytes of backed up CMOS RAM, of which 14 bytes containing the RTC time and date information, and RTC configuration. During power-down, the RTC consumes 0.9uA/hr. The optional power-down backup method uses a Super CAP with a 1 Farad capacity. This provides 300 hours of RTC/SRAM backup. The default battery is an external +3V lithium battery with a capacity of 200mAh, which provides three years of backup.

5.18 Single Width Mid-size AMC

ATCA-7367 supports one slot of single width mid-size AMC to extend the application range of the blade by adding appropriate cards. This can be straight forward storage and network interface solutions or local storage hosted on an AMC. However it is also necessary to address applications requiring intelligent solutions that can handle tasks like TCP/IP off load, IPv4 and IPv6 stacks, unicast/multicast routing acceleration, IPSEC acceleration, firewall, SRTP offload, transport protocols, and mobile-IP, among others.

6.1 Interrupt Structure

The ATCA-7367 supports NON-APIC (legacy PIC Mode) and APIC mode of Interrupt delivery to the CPUs. The 8259 PIC Mode Interrupt Concentrator inside the ICH10R supports 16 interrupts (eight external signal inputs). The IO-APIC device inside the ICH10R supports 24 interrupt sources. In APIC mode the ICH10R supports only Front side bus interrupt delivery (not the serial APIC mode). The following figure and tables summarize the interrupt sources and mappings for ATCA-7367. APIC mode is configured through BIOS after boot-up phase which is done in legacy PIC mode.

Figure 6-1 Interrupt Structure on ATCA-7367

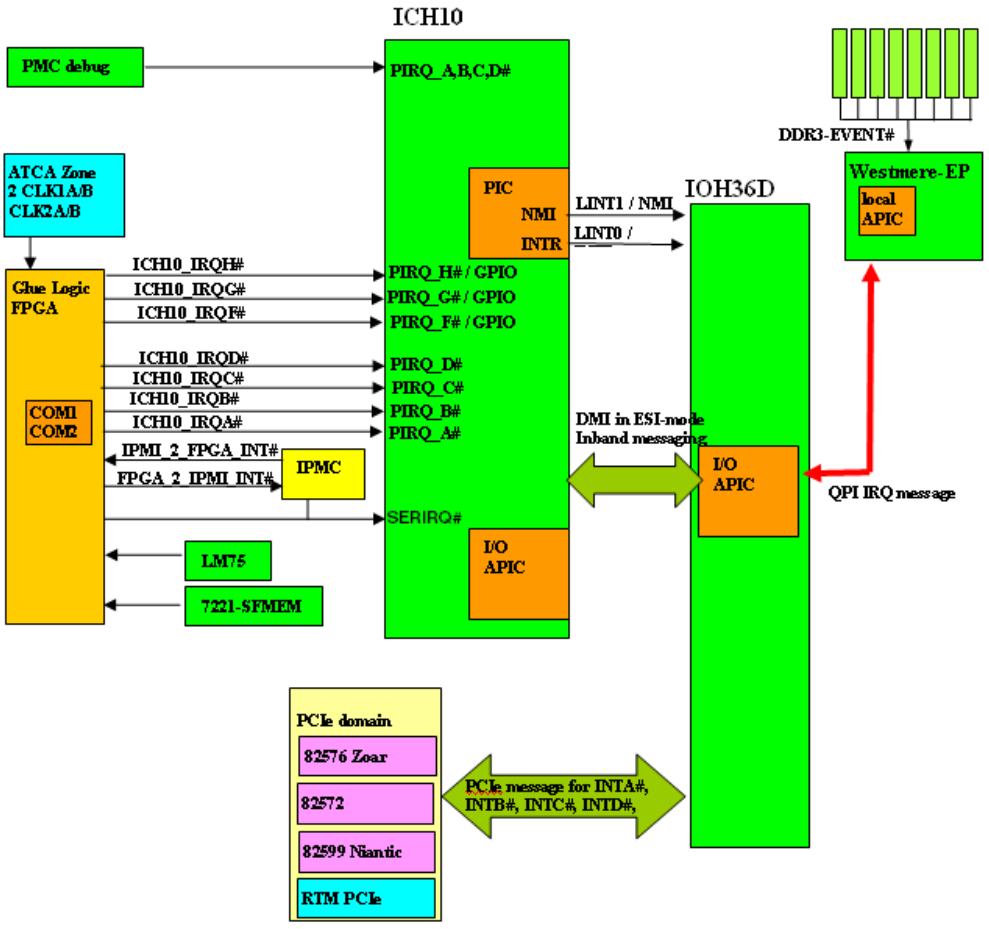


Table 6-1 Non-APIC (PIC mode / 8259 Mode) Interrupt Mapping

	8259 IRQ	Typical Interrupt Source	Interrupt Source
Master	0	Internal	8254 Counter 0, Timer 0 (HPET)
	1	Keyboard	IRQ1 via SERIRQ
	2	Internal	Slave 8259 INTR output
	3	Serial Port A	IRQ3 via SERIRQ, PIRQ#
	4	Serial Port B	IRQ4 via SERIRQ, PIRQ#
	5	Parallel/Generic	IRQ5 via SERIRQ, PIRQ#
	6	Floppy	IRQ6 via SERIRQ, PIRQ#
	7	Parallel/Generic	IRQ7 via SERIRQ, PIRQ#
Slave	8	Internal RTC	Internal RTC, Timer 1 (HPET)
	9	Generic	IRQ9 via SERIRQ, SCI, TCO, or PIRQ#
	10	Generic	IRQ10 via SERIRQ, SCI, TCO, or PIRQ#
	11	Generic	IRQ11 via SERIRQ, SCI, TCO, or PIRQ# or Timer#2 (HPET)
	12	PS/2 Mouse	IRQ11 via SERIRQ, SCI, TCO, or PIRQ# or Timer#3 (HPET)
	13	Internal	State Machine output based on processor FERR# assertion. May optionally be used for SCI or TCO interrupt if FERR# not needed.
	14	SATA	SATA Primary (legacy mode), or via SERIRQ or PIRQ#
	15	SATA	SATA Secondary (legacy mode), or via SERIRQ or PIRQ#

IRQ0,1,2,8 and 13 must not be used for PCI Interrupts (external inputs PIRQ [A...H]#) routing. If an Interrupt is used for PCI IRQ [A:H], SCI or TCO, it must not be used for ISA (legacy)-style Interrupts (via SERIRQ). In PIC Mode (8259.mode), PCI Interrupts are mapped to IRQ3-7,9-12, 14 or 15. If IRQ11 is used for Timer 2, software must ensure IRQ11 is not shared with any other devices to guarantee the proper operation of Timer 2. TheICH10R does not prevent the sharing of IRQ11. Interrupts can individually be programmed to be edge or level, except for IRQ0, IRQ2, IRQ8#, and IRQ13.

Table 6-2 APIC Mode Interrupt Mapping

IRQ	Interrupt Source
0	Cascade from 8259 1
1	
2	8254 Counter 0, Timer 0 (legacy mode)
3	
4	
5	
6	
7	
8	RTC, Timer 1 (legacy mode)
9	Option for TCI, TCO
10	Option for TCI, TCO
11	Timer 2, Option for TCI, TCO
12	Timer 3
13	FERR# logic
14	SATA Primary (legacy mode)
15	SATA Secondary (legacy mode)
16	PIRQ[A]#
17	PIRQ[B]#
18	PIRQ[C]#
19	PIRQ[D]#
20	PIRQ[E]# (GPIO)
21	PIRQ[F]# (GPIO)
22	PIRQ[G]# (GPIO)
23	PIRQ[H]# (GPIO)

In APIC mode the PCI Interrupts A:H are mapped to IRQ[16:23].

If an Interrupt is used for PCI IRQ[A:H], SCI or TCO it must not be used for ISA (legacy)-style interrupts (via SERIRQ).

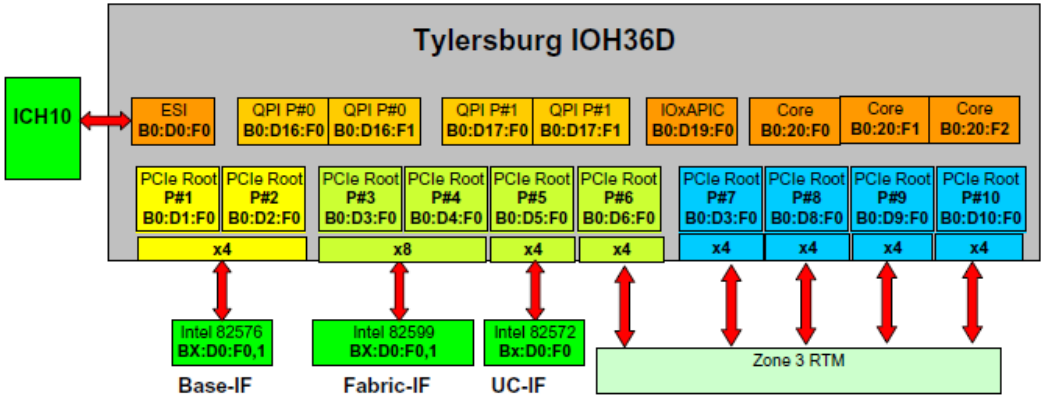
6.2 PCI Express Port Mapping

Xeon 5520 (Tylersburg IOH36 D) PCIexpress ports have the naming convention as seen in Figure "IOH36D PCIe Port Mapping on ATCA-7367" on page 138.

Table 6-3 PCIexpress Port Mapping

Port#	1	2	3	4	5	6	7	8	9	10
	x2	x2	x4	x4	x4	x4	x4	x4	x4	x4
	x4		x8		x8		x8		x8	
			x16				x16			

Figure 6-2 IOH36D PCIe Port Mapping on ATCA-7367

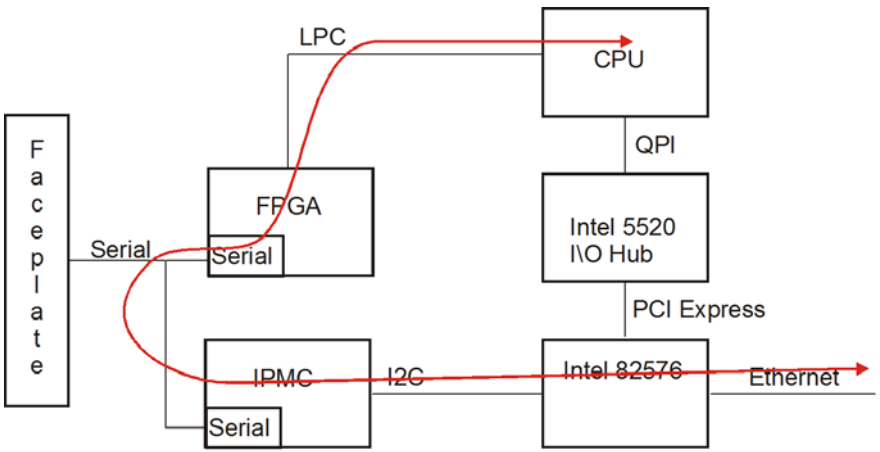


7.1 Overview

Serial Over LAN (SOL) is a mechanism that you can use to redirect the serial console from the blade via an IPMI session over the network. SOL uses the RMCP+ protocol.

The IPMC is used to establish and control the SOL session. SOL is only available on the base interface. The sideband interface of the Intel 82576 (in pass-through mode) is used to transmit/receive its terminal characters via the base interface.

Figure 7-1 SOL Overview



You can configure the SOL parameters using the standard IPMI commands or via an open source tool called "ipmitool".

7.2 Installing the ipmitool

You can download the open source tool ipmitool from http://ipmitool.sourceforge.net (at the time of publishing this manual the current version is 1.8.10). Documentation for this tool is also freely available on this site.

Procedure

To install the ipmitool, proceed as follows:

1. Download the ipmitool tar file from http://ipmitool.sourceforge.net to your blade.
2. Extract the source code.
   `prompt>tar -xjvf ipmitool-<version>.tar.bz2`
3. Go to the directory to which you have extracted the ipmitool.
   `prompt>cd <path>/ipmitool-<version>`
4. Build the ipmitool.
   `prompt>./configure && make && make install`

7.3 Configuring SOL Parameters

You can configure the following SOL parameters.

Table 7-1 SOL Parameters

Parameter	Description
Set LAN Configuration Parameter (IP address/MAC address)	Use this command to set the IP and MAC address.
Set Channel Access (Privilege level)	Use this command to set the privilege level.
Set User Name	Default value is soluser.
Set User Password	Default value is solpasswd.

You can use standard IPMI commands or the ipmitool to modify the parameters.

7.3.1 Using Standard IPMI Commands

This example shows how to set up the SOL configuration parameter with standard IPMI commands. Ipmicmd is used on the local IPMC and the IP is configured.

Sample Procedure

To set the IP address, proceed as follows:

1. Establish an IPMI connection to the blade.
2. Set LAN Configuration Parameter Set In Progress Lock.
   ipmicmd -k "f 0 c 1 5 0 1" smi 0
3. Set LAN Configuration Parameter Set IP (172.16.10.11 on channel 5).
   ipmicmd -k "f 0 c 1 5 3 ac 10 0a 0b" smi 0
4. Set LAN Configuration Parameter Set In Progress Commit.
   ipmicmd -k "f 0 c 1 5 0 2" smi 0

7.3.2 Using ipmitool

The example below shows how to setup a LAN configuration parameter for a potential SOL session with ipmitool for base 1 (channel 5).

```
n0s70:~ #ipmitool lan set 5 ipaddr 172.16.0.221

Setting LAN IP Address to 172.16.0.221

n0s70:~ #
```

The following example shows how to query the LAN parameters that are currently in use for a potential SOL session for base 1(channel 5) and base 2(channel 6):

```
root@localhost:~# ipmitool lan print 5

Set in Progress         : Set Complete

Auth Type Support       :

Auth Type Enable        : Callback :

                        : User     :

                        : Operator :

                        : Admin    :
```

```
                          : OEM      :
IP Address Source         : Unspecified
IP Address                : 172.16.0.221
Subnet Mask               : 255.255.0.0
MAC Address               : 00:00:00:00:00:00
Default Gateway IP        : 172.16.0.1
Default Gateway MAC       : 00:00:00:00:00:00
RMCP+ Cipher Suites       : 1,2,3,3
Cipher Suite Priv Max     : Not Available
root@localhost:~# ipmitool lan print 6
Set in Progress           : Set Complete
Auth Type Support         :
Auth Type Enable          : Callback :
                          : User     :
                          : Operator :
                          : Admin    :
                          : OEM      :
IP Address Source         : Unspecified
IP Address                : 172.17.1.220
Subnet Mask               : 255.255.0.0
MAC Address               : 00:00:00:00:00:00
Default Gateway IP        : 172.17.0.1
Default Gateway MAC       : 00:00:00:00:00:00
```

```
RMCP+ Cipher Suites     : 1,2,3,3

Cipher Suite Priv Max   : Not Available

root@localhost:~#
```

MAC Address 00:00:00:00:00:00 means the address is shared between base and SOL interface. The address can be found out in the MAC address record of the FRU.

7.4 Establishing a SOL Session

To start a SOL session, the following requirements must be fulfilled:

- An Ethernet LAN connection to the 82576 controller of the ATCA-7367 must exist.
- ATCA-7367 IPMC FW must correspond to version 2.00.7 and above.

Procedure

To establish a SOL session, proceed as follows.:

1. Make sure that the requirements detailed above are fulfilled.
2. Compile and install the ipmitool on your target which is destined for opening the SOL session on the ATCA-7367. For details refer to *Installing the ipmitool* on page 139.
3. Apply an IP address to the ATCA-7367 SOL interface. For details refer to *Configuring SOL Parameters* on page 140.
4. If necessary change user and password.
   Default user is "soluser" and password is "solpasswd".
5. Configure the network between the ATCA-7367 and your target, which is destined for opening the SOL session, so that the SOL IP address is accessible.

6. Start ATCA-7367 SOL session on your target with the ipmitool and the configured IP address for the ATCA-7367 SOL interface.
   `ipmitool -C 1 -I lanplus -H 172.16.0.221 -U soluser -P solpasswd -k gkey sol activate`
   For details on the command parameters, refer to the ipmitool documentation available on http://ipmitool.sourceforge.net.

To access BIOS setup screen, it is necessary to reset the payload. SOL session is only available if the payload is powered on and initialized by the BIOS.

Supported IPMI Commands

8.1 Standard IPMI Commands

The IPMC is fully compliant to the Intelligent Platform Management Interface v.1.5. This section provides information about the supported IPMI commands.

8.1.1 Global IPMI Commands

The IPMC supports the following global IPMI commands.

Table 8-1 Supported Global IPMI Commands

Command	NetFn (Request/Response)	CMD	Comments
Get Device ID	0x06/0x07	0x01	-
Cold Reset	0x06/0x07	0x02	-
Warm Reset	0x06/0x07	0x03	-
Get Self Test Results	0x06/0x07	0x04	-
Get Device GUID	0x06/0x07	0x08	-
Master Write-Read	0x06/0x07	0x52	Only for accessing private I2C buses.

8.1.2 System Interface Commands

The system interface commands are supported by blades providing a system interface.

Table 8-2 Supported System Interface Commands

Command	NetFn (Request/Response)	CMD
Set BMC Global Enables	0x06/0x07	0x2E
Get BMC Global Enables	0x06/0x07	0x2F
Clear Message Flags	0x06/0x07	0x30
Get Message Flags	0x06/0x07	0x31
Get Message	0x06/0x07	0x33
Send Message	0x06/0x07	0x34

Table 8-2 Supported System Interface Commands (continued)

Command	NetFn (Request/Response)	CMD
Set Channel Access	0x06/0x07	0x40
Get Channel Access	0x06/0x07	0x41
Get Channel Info	0x06/0x07	0x42
Set User Access	0x06/0x07	0x43
Get User Access	0x06/0x07	0x44
Set User Name	0x06/0x07	0x45
Get User Name	0x06/0x07	0x46
Set User Password	0x06/0x07	0x47
Set User Payload Access	0x06/0x07	0x4C
Get User Payload Access	0x06/0x07	0x4D
Set Channel Security Keys	0x06/0x07	0x5C

8.1.3 Watchdog Commands

The watchdog commands are supported by blades providing a system interface and a watchdog type 2 sensor.

The options pre-timeout and power-cycle are not supported.

Table 8-3 Supported Watchdog Commands

Command	NetFn (Request/Response)	CMD
Reset Watchdog Timer	0x06/0x07	0x22
Set Watchdog Timer	0x06/0x07	0x24
Get Watchdog Timer	0x06/0x07	0x25

8.1.4 SEL Device Commands

Table 8-4 Supported SEL Device Commands

Command	NetFn (Request/Response)	CMD
Get SEL Info	0x0A/0x0B	0x40
Reserve SEL	0x0A/0x0B	0x42
Get SEL Entry	0x0A/0x0B	0x43
Add SEL Entry	0x0A/0x0B	0x44
Clear SEL	0x0A/0x0B	0x47
Get SEL Time	0x0A/0x0B	0x48
Set SEL Time	0x0A/0x0B	0x49

8.1.5 FRU Inventory Commands

Table 8-5 Supported FRU Inventory Commands

Command	NetFn (Request/Response)	CMD
Get FRU Inventory Area Info	0x0A/0x0B	0x10
Read FRU Data	0x0A/0x0B	0x11
Write FRU Data	0x0A/0x0B	0x12

8.1.6 Sensor Device Commands

Table 8-6 Supported Sensor Device Commands

Command	NetFn (Request/Response)	CMD	Comments
Get Device SDR Info	0x04/0x05	0x20	-
Get Device SDR	0x04/0x05	0x21	-
Reserve Device SDR Repository	0x04/0x05	0x22	-
Get Sensor Reading Factors	0x04/0x05	0x23	-
Set Sensor Hysteresis	0x04/0x05	0x24	-
Get Sensor Hysteresis	0x04/0x05	0x25	-
Set Sensor Threshold	0x04/0x05	0x26	Most of the threshold-based sensors have fixed thresholds. Before using this command, check whether threshold setting is supported by using the Get Device SDR command.
Get Sensor Threshold	0x04/0x05	0x27	-
Set Sensor Event Enable	0x04/0x05	0x28	-
Get Sensor Event Enable	0x04/0x05	0x29	-
Get Sensor Event Status	0x04/0x05	0x2B	-
Get Sensor Reading	0x04/0x05	0x2D	-
Get Sensor Type	0x04/0x05	0x2F	-
Set Event Receiver	0x04/0x05	0x00	-
Get Event Receiver	0x04/0x05	0x01	-
Platform Event	0x04/0x05	0x02	-

8.1.7 Chassis Device Commands

Table 8-7 Supported Chassis Device Commands

Command	NetFn (Request/Response)	CMD
Set System Boot Options	0x00/0x01	0x08
Get System Boot Options	0x00/0x01	0x09

8.1.7.1 System Boot Options Commands

The IPMI system boot options commands allow you to control the boot process of a blade by sending boot parameters to the blade's boot firmware (for example BIOS, U-Boot or VxWorks). The boot firmware interprets the sent boot parameters and executes the boot process accordingly. Each boot parameter addresses a particular functionality and consists of a sequence of one or more bytes. The IPMI specification assigns numbers to boot parameters. Boot parameters 0 to 7 are standard parameters whose structure and functionality is defined by the IPMI specification. The boot parameters 96 to 127 are OEM-specific which can be used for different purposes.

When using the Get/Set System Boot Options commands, except for parameter 100, use the response/request data fields with the Set Selector and the Block Selector set to 0x00. When using the Get/Set System Boot Option for the parameter 100, the Set Selector and the Block Selector have a specific meaning. Details are given in *System Boot Options Parameter #100* on page 152 for details.

The following table lists which boot properties can be configured and the corresponding boot parameter number.

Table 8-8 Configurable System Boot Option Parameters

Configurable Boot Property	Corresponding Boot Parameter Number
Selection between default and backup boot flash as device to boot from	96
POST Type	97
Timeout for graceful shutdown	98

Table 8-8 Configurable System Boot Option Parameters (continued)

Configurable Boot Property	Corresponding Boot Parameter Number
BIOS boot parameters as defined in Table 8-15 on page 156	100

8.1.7.1.1 System Boot Options Parameter #96

This boot parameter is an Artesyn-specific OEM boot parameter. Its definition is given in the following table.

Table 8-9 System Boot Options Parameter #96

Data Byte	Description
1	Bits 7..1: Reserved Bit 0: Default/backup boot flash selection 0: Boot from default boot flash 1: Boot from backup boot flash Note: the newly selected boot flash is connected to the payload immediately, that means writing to the flash is possible. Its image is executed after the next power-up or cold reset of the payload.

The System Boot Options parameter #96 is non-volatile. During blade production, its data is initialized to 0xFF and its state is set to invalid. Its parameter data remains preserved after IPMC power cycles and firmware upgrades.

8.1.7.1.2 System Boot Options Parameter #97

This boot parameter is an Artesyn-specific OEM parameter. Its definition is given in the following table.

Table 8-10 System Boot Options Parameter #97

Data Byte	Description
1	POST Type Data 1 - Set Selector. This is the processor ID for which the boot option is to be set.
2	Data 2 - POST Type Selector. This parameter is used to specify the POST type that the IPMC will execute. 0x00: Short POST 0x01: Long POST 0x02 to 0xFF: Not used

The System Boot Options parameter #97 is non-volatile. During blade production, its data is initialized to 0xFF and its state is set to invalid. Its parameter data remains preserved after IPMC power cycles and firmware upgrades.

8.1.7.1.3 System Boot Options Parameter #98

This boot parameter is an Artesyn-specific OEM parameter.

This timer specifies how long the IPMC waits for the payload to shut down gracefully. If the payload software does not configure its OpenIPMI library to be notified for graceful shutdown requests, the IPMC shuts down the payload when the timer expires.

Table 8-11 System Boot Options Parameter #98

Bit	Description
15:8	Timeout for GRACEFUL_SHUTDOWN, LSB (given in 100 msec)
7:0	Timeout for GRACEFUL_SHUTDOWN, MSB (given in 100 msec)

The System Boot Options parameter #98 is non-volatile. During blade production its data is initialized to 0xFF and its state is set to invalid. Its parameter data remains preserved after IPMC power cycles and firmware upgrades.

8.1.7.1.4 System Boot Options Parameter #100

The system boot options parameter #100 allows you to send multiple boot options to the blade's boot firmware and thus control the boot process. The boot options which you can configure using this parameter are typically a subset of the boot options which you can configure in the boot firmware directly, for example, using a setup menu. Details are given in this section.

The IPMC contains a storage area where the boot parameters are stored. When the blade boots, the boot firmware reads out the storage area, interprets the parameters and executes the boot process accordingly. Note that the boot parameters in the IPMC storage area have higher priority than the same boot options which may be configured in the firmware itself, for example, using the setup menu.

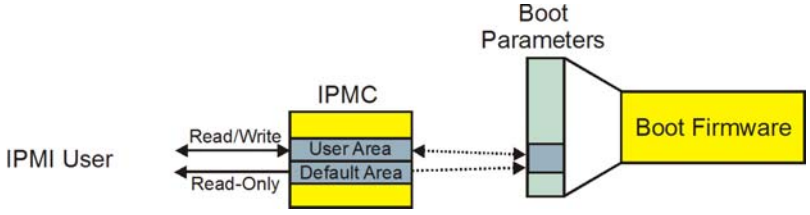
The storage area is divided into two parts: the default area and the user area. The user area can be read and written by an IPMI user and, by default, is the area which the boot firmware reads out and uses during the boot process. The default area can only be read (by both the IPMI user and the boot firmware.). Its purpose is to store factory-programmed default boot options which can be used to restore the standard settings. If you want the boot firmware to read out

and use the boot parameters stored in the default area and thus use the factory settings, you need to configure the blade accordingly. This is typically done by an on-board switch (for example, “Clear CMOS RAM”). It depends on the blade and firmware which settings are stored in the default area. Details are given in the following sections.

On some blades with particular firmware types, changing a boot parameter in the firmware setup menu changes the boot parameter in the user area as well, if the same parameter is defined both in the user area and the set-up menu. Details are given below.

The following figure summarizes the previously explained basic information flow related to the system boot options parameter #100.

Figure 8-1 System Boot Options Parameter #100 - Information Flow Overview



The boot options need to be stored as a sequence of zero terminated strings. The following table describes in detail the format of the boot options to be used when setting or reading the System Boot Options parameter #100.

Table 8-12 System Boot Options - Parameter #100 - Data Format

Byte	Description
0..1	Number of bytes used for boot parameters (LSB first) The number of bytes must be calculated and written into these two bytes by the software which writes into the storage area. The values 0x0000 and 0xFFFF indicate that no data has been written to the storage area. When reading from the storage area and you find any of these two values, your software should assume that no user-specific boot options have previously been written to the storage area.

Table 8-12 System Boot Options - Parameter #100 - Data Format (continued)

Byte	Description
2 .. n	Boot parameters data The boot parameters are stored as ASCII text with the following general format: <name>=<value>, where all name/value pairs are separated by a zero byte. The end of the boot parameter data is indicated by two zero bytes. Allowed and supported name/value pairs are blade-specific. Details are given below.
n + 1 .. n + 2	16 byte checksum over the boot parameters data section. (LSB first) For backward compatibility reasons, the checksums 0x0000 and 0xFFFF are accepted as valid. They indicate that no checksum has been calculated and stored.

When writing to or reading from the storage area, you can only read or write chunks of 16 bytes at a time. For this reason, the default and user area are divided into numbered blocks of 16 bytes which need to be addressed individually. For this purpose, the “Block Selector” field in the request data field is used. The “Set Selector” field, on the other hand, is used to select either the default or user area. The following two tables describe in detail how the request and response data fields need to be filled and interpreted when performing SET and GET accesses.

Table 8-13 System Boot Options Parameter #100 - SET Command Usage

Byte	Description
Request Data	
1	Bit 7: when set to "1", the storage area on the IPMC is locked, i.e. no other software can access it. This should be set, before doing any modifications and cleared again after the final access. Bits 6..0: must contain the value: "100" indicating this OEM system boot option.
2	Set Selector Must be set to "0" (user area). You can only write to the user area, therefore no other values are supported.
3	Block Selector Zero based index of the 16-byte block which you want to write to. Index 0 refers to the first block of 16 bytes, which includes the first two bytes that indicate the boot parameter data size. Depending on the total length of the boot option data, your software may need to write several blocks of 16 bytes in a row, each individually addressed using the block selector.

Table 8-13 System Boot Options Parameter #100 - SET Command Usage (continued)

Byte	Description
4 .. n (n <= 19)	Data that you want to write into the addressed block. This will be a chunk of the boot parameter data. If less than 16 bytes are written, then only the provided data is written, the remaining bytes in the addressed storage area block are left unchanged.
Response Data	
1	0x00: Write successful 0x80: Boot parameter storage not supported by the IPMC 0x81: Storage area is locked by another software entity 0x82: Illegal write-access 0xC9: Block selector is outside of the allowed range.

Table 8-14 System Boot Options Parameter #100 - GET Command Usage

Byte	Description
Request Data	
1	Bit 7: reserved. Set to "0". Bits 6..0: must contain the value:" 100", indicating this OEM system boot option.
2	Set Selector 0: User area 1: Default area
3	Block Selector Zero based index of the 16-byte block which you want to read from. Index 0 refers to the first block of 16 bytes, which includes the first two bytes which indicate the boot parameter data size.
Response Data	
1	0x00: Read successful 0x80: Boot parameter storage not supported by the IPMC 0xC9: Block selector is outside of the allowed range.
2	Reserved. Set to "1".
3	Bit 7: If set to "1", the addressed storage area is locked. Bits 6 ..0: value "100", indicating this OEM boot option command.

Table 8-14 System Boot Options Parameter #100 - GET Command Usage (continued)

Byte	Description
4 .. 19	The content of the read 16-byte block.

In order to detect the maximum size of writable storage area, your software can perform a series of read accesses while incrementing the block selector with each access. Once the error code C9 is returned, the limit has been reached and the total available space in the writable storage area can be easily determined by the number of previously performed successful read accesses.

This is supported by HPI, for details refer to the *System Management Interface Based on HPI-B User's Guide* related to your system environment.

The following table lists boot parameters which can be configured for the ATCA-7367 blade, using the system boot option parameter #100.

Artesyn Embedded Technologies provides the tool "ipmibpar" to interpret the ASCII parameters. To obtain the tool, contact your local sales representative.

When used in the System Boot Options parameter #100, the boot parameters and their values are case-sensitive.

All boot options listed in the following table are set by the BIOS setup menu and can be configured using the System Boot options command #100. The IPMC and BIOS software automatically synchronize the settings made in the BIOS setup menu and the settings specified using the System Boot Options command #100. Changing a parameter in either of these, automatically changes the respective value in the other.

Table 8-15 System Boot Options Parameter #100 - Supported Parameters

Parameter	Description	Values
baudrate	Console baud rate	9600/19200/57600/115200

Table 8-15 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Description	Values
usb	USB support	fp_on/fp_off,rtm_on/rtm_off,onboard_on/onboard_off Example: usb=fp_off,rtm_off,onboard_on -> Front panel USB off, RTM USB off, Onboard Flash USB on
os_boot_watchdog	OS boot Watchdog (IPMI)	on/off,timout in minutes,action Timeout range 1,2,3,5,7,10,15,20 action: noaction/reset,poweroff, Example: os_boot_watchdog=on,10,reset -> watchdog is on, 10 minutes timeout, action=reset
frontnet_boot	Boot from Front Panel Network	off/on
basenet_boot	Boot from Base Network	off/on
artm_net_boot	Boot from ARTM Network	off/on
artm_sas_boot	Boot from ARTM SAS device	off/on
artm_fc_boot	Boot from ARTM FC device	off/on
hyper_threading	Enable/disable hyper-threading	on/off
turbo_mode	Enable/disable turbo mode	on/off
post_watchdog	Post Watchdog (IPMI)	On/off,timeout in minutes,action Timeout range 3,4,5,5 action: noaction/reset,poweroff, Example: post_watchdog=on,5,reset -> watchdog is on, 5 minutes timeout, action=reset

Table 8-15 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Description	Values
rtm_auto	Auto detection of RTM	on/off: auto detect on/off gen1on/gen1off: Force Gen1 on/off x4x4x4x4/x4x4x8/x8x4x4/x8x8/x16: PCIe bifurcation Examples: rtm_auto=off,gen1on,x4x4x8 -> RTM auto detect off, Gen1 on, PCIe x4x4x8 rtm_auto=on,gen1on,x4x4x8 -> RTM auto detect on, ignore other parameter
boot_order	Boot priority order	device1,devcice2,..device8 See *boot_order Devices*

Table 8-16 boot_order Devices

Device	Description
sata0	SATA device 0 (Debug SATA)
sata1	SATA device 1 (RTM Debug SATA)
sata5	SATA device 5 (Onboard SATA)
sataonboard	SATA device 5 (Onboard SATA)
sashdd	SAS HDD mounted on the RTM
sas0_nn	SAS Controller nn = SCSI ID (use this when a SAS array is connected to the RTM)
frontnet	Front Panel Network
basenet0	Base0 Network
basenet1	Base1 Network
usb1	USB frontpanel 1
usb2	USB frontpanel 2
usbonboard	USB onboard HDD
usbartm	USB artm
usbkey	USB key

Table 8-16 boot_order Devices (continued)

Device	Description
usbcdrom	USB cdrom
usbhdd	USB hdd
usbfdd	USB floppy disk
efishell	Built in UEFI shell
Up to 8 boot devices are supported. Example: boot_order=sas0_03,basenet0,usbkey,sata1	

8.1.8 LAN Device Commands

Table 8-17 Supported LAN Device Commands

Command	NetFn (Request/Response)	CMD
Set LAN Configuration Parameters	0x0C/0x0D	0x01
Get LAN Configuration Parameters	0x0C/0x0D	0x02
Set SOL Configuration Parameters	0x0C/0x0D	0x21
Get SOL Configuration Parameters	0x0C/0x0D	0x22

8.2 PICMG 3.0 Commands

The Artesyn Embedded Technologies IPMC is a fully compliant AdvancedTCA intelligent Platform Management Controller. it supports all required and mandatory AdvancedTCA commands as defined in the PICMG 3.0 and AMC.0 R2.0 specifications.

Table 8-18 Supported PICMG 3.0 Commands

Command	NetFn (Request/Response)	CMD	Comments
Get PICMG Properties	0x2C/0x2D	0x00	-
Get Address Info	0x2C/0x2D	0x01	-
FRU Control	0x2C/0x2D	0x04	The blade supports the cold reset and graceful reboot options.
Get FRU LED Properties	0x2C/0x2D	0x05	-
Get FRU LED Color Capabilities	0x2C/0x2D	0x06	-
Set FRU LED State	0x2C/0x2D	0x07	-
Get FRU LED State	0x2C/0x2D	0x08	-
Set IPMB State	0x2C/0x2D	0x09	-
Set FRU Activation Policy	0x2C/0x2D	0x0A	-
Get FRU Activation Policy	0x2C/0x2D	0x0B	-
Set FRU Activation	0x2C/0x2D	0x0C	-
Get Device Locator Record ID	0x2C/0x2D	0x0D	The Artesyn Embedded Technologies IPMCs support the standard PICMG 3.0 and the extended AMC.0 R2.0 versions of this command.
Set Port State	0x2C/0x2D	0x0E	-
Get Port State	0x2C/0x2D	0x0F	-
Compute Power Properties	0x2C/0x2D	0x10	-
Set Power Level	0x2C/0x2D	0x11	-
Get Power Level	0x2C/0x2D	0x12	-

Table 8-18 Supported PICMG 3.0 Commands (continued)

Command	NetFn (Request/Response)	CMD	Comments
Get IPMB Link Info	0x2C/0x2D	0x18	-
Set AMC Port State	0x2C/0x2D	0x19	-
Get AMC Port State	0x2C/0x2D	0x1A	-
Get FRU Control Capabilities	0x2C/0x2D	0x1E	-
Get target upgrade capabilities	0x2C/0x2D	0x2E	-
Get component properties	0x2C/0x2D	0x2F	-
Abort firmware upgrade	0x2C/0x2D	0x30	-
Initiate upgrade action	0x2C/0x2D	0x31	-
Upload firmware block	0x2C/0x2D	0x32	-
Finish firmware upload	0x2C/0x2D	0x33	-
Get upgrade status	0x2C/0x2D	0x34	-
Activate firmware	0x2C/0x2D	0x35	-
Query self-test results	0x2C/0x2D	0x36	-
Query rollback status	0x2C/0x2D	0x37	-
Initiate manual rollback	0x2C/0x2D	0x38	-

The firmware upgrade commands supported by the blade are implemented according to the PICMG HPM.1 Revision 1.0 specification.

The boot block can be updated with PICMG HPM.1 specific commands.

8.2.1 Set/Get Power Level

The blade supports two power levels. In case of a shelf which only allows 116 W per slot the P-States of the blade will be restricted to match this requirement. The second power level has no restrictions.

For more information, refer to Chapter 4, *BIOS, on page 77*.

8.3 Artesyn Embedded Technologies Specific Commands

The Artesyn Embedded Technologies IPMC supports several commands which are not defined in the IPMI or PICMG 3.0 specification but are introduced by Artesyn Embedded Technologies: serial output commands.

- Before sending any of these commands, the shelf management software must check whether the receiving IPMI controller supports Artesyn Embedded Technologies specific IPMI commands by using the IPMI command 'Get Device ID'. Sending Artesyn Embedded Technologies specific commands to IPMI controllers which do not support these IPMI commands will lead to no or undefined results.
- Proper handling of these commands is required to write a portable application.

8.3.1 Set/Get Feature Configuration

ATCA-7367 provides an OEM command to control the SAS signal which routes from the RTM.

Table 8-19 Set/Get Feature Configuration

Command Name	NetFn (Request/Response)	CMD	Description
Set Feature Configuration	0x2E/0x2F	0x1E	
Get Feature Configuration	0x2E/0x2F	0x1F	

8.3.1.1 Set Feature Configuration (0x1E)

This command is used to switch SAS signal to AMC or Update Channel.

Table 8-20 Set Feature Configuration Command

	Byte	Data Field
Request Data	1	LSB of Artesyn IANA Enterprise Number. A value of CDh shall be used.
	2	2nd byte of Artesyn IANA Enterprise Number. A value of 65h shall be used.
	3	MSB of Artesyn IANA Enterprise Number. A value of 00h shall be used.
	4	Feature Selector. E0h = SAS Signal Switch for AMC or Update Channel
	5	Feature Configuration 00h = SAS to Zone 2 update channel 01h = SAS to AMC(Default) 02h = restore factory default
	6	Persistency / Duration FFh = persistent over power cycle (default)
Response Data	1	Completion Code. Generic plus the following command-specific completion codes: 80h = feature selector not supported. 81h = feature configuration not supported 82h = configuration persistency / duration not supported
	2	LSB of Artesyn IANA Enterprise Number. A value of CDh shall be used.
	3	2nd byte of Artesyn IANA Enterprise Number. A value of 65h shall be used.
	4	MSB of Artesyn IANA Enterprise Number. A value of 00h shall be used.

8.3.1.2 Get Feature Configuration (0x1F)

This command can be used to retrieve the IPMI feature set being configured.

Table 8-21 Get Feature Configuration Command

	Byte	Data Field
Request Data	1	LSB of Artesyn IANA Enterprise Number. A value of CDh shall be used.
	2	2nd byte of Artesyn IANA Enterprise Number. A value of 65h shall be used.
	3	MSB of Artesyn IANA Enterprise Number. A value of 00h shall be used.
	4	Feature Selector, a value of 0xE0 shall be used. 0xE0h = SAS Switch for AMC or Update Channel
Response Data	1	Completion Code. Generic plus the following command-specific completion codes: 80h = feature selector not supported.
	2	LSB of Artesyn IANA Enterprise Number. A value of CDh shall be used.
	3	2nd byte of Artesyn IANA Enterprise Number. A value of 65h shall be used.
	4	MSB of Artesyn IANA Enterprise Number. A value of 00h shall be used.
	5	Feature Configuration 00h = SAS to Zone 2 update channel 01h = SAS to AMC
	6	Persistency / Duration FFh = persistent over power cycle

8.3.2 Serial Output Commands

Table 8-22 Serial Output Commands

Command Name	NetFn (Request/Response)	CMD	Description
Set Serial Output	0x2E/0x2F	0x15	See *Set Serial Output Command* on page 165
Get Serial Output	0x2E/0x2F	0x16	See *Get Serial Output Command* on page 166

8.3.2.1 Set Serial Output Command

The Set Serial Output command selects the serial port output source for a serial port connector.

8.3.2.1.1 Request Data

The following table lists the request data applicable to the Set Serial Output command.

Table 8-23 Request Data of Set Serial Output Command

Byte	Data Field
1	LSB of Artesyn Embedded Technologies IANA Enterprise number. A value of 0xCD has to be used.
2	Second byte of Artesyn Embedded Technologies IANA Enterprise number. A value of 0x65 has to be used.
3	MSB of Artesyn Embedded Technologies IANA Enterprise number. A value of 0x00 has to be used.
4	Serial connector type 0: Face plate connector 1: Backplane connector All other values are reserved. Note: Only the faceplate connector is supported. No connector on the RTM available.
5	Serial connector instance number. A sequential number that starts from "0".

Table 8-23 Request Data of Set Serial Output Command (continued)

Byte	Data Field
6	Serial output selector 0: BIOS 2: IPMC debug console All other values are reserved.

8.3.2.1.2 Response Data

The following table lists the response data applicable to the Set Serial Output command.

Table 8-24 Response Data of Set Serial Output Command

Byte	Data Field
1	Completion code
2	LSB of Artesyn Embedded Technologies IANA Enterprise number.
3	Second byte of Artesyn Embedded Technologies IANA Enterprise number.
4	MSB of Artesyn Embedded Technologies IANA Enterprise number.

8.3.2.2 Get Serial Output Command

The Get Serial Output Command provides a way to determine which serial output source goes to a particular serial port connector.

Currently, only BIOS output is supported.

8.3.2.2.1 Request Data

The following table lists the request data applicable to the Get Serial Output command.

Table 8-25 Request Data of Get Serial Output Command

Byte	Data Field
1	LSB of Artesyn Embedded Technologies IANA Enterprise number. A value of 0xCD has to be used.
2	Second byte of Artesyn Embedded Technologies IANA Enterprise number. A value of 0x65 has to be used.
3	MSB of Artesyn Embedded Technologies IANA Enterprise number. A value of 0x00 has to be used.
4	Serial connector type 0: Face plate connector 1: Backplane connector All other values are reserved. Note: Only the faceplate connector is supported. No connector on the RTM available.
5	Serial connector instance number. A sequential number that starts from "0".

8.3.2.2.2 Response Data

The following table lists the response data applicable to the Get Serial Output command.

Table 8-26 Response Data of Get Serial Output Command

Byte	Data Field
1	Completion code
2	LSB of Artesyn Embedded Technologies IANA Enterprise number.
3	Second byte of Artesyn Embedded Technologies IANA Enterprise number.
4	MSB of Artesyn Embedded Technologies IANA Enterprise number.
5	Serial output selector

8.4 Pigeon Point Specific Commands

The IPMC supports additional IPMI commands that are specific to Pigeon Point. This section provides detailed descriptions of those extensions:

Table 8-27 Pigeon Point Extension Commands

Command	NetFn (Request/Response)	CMD
Get Status Table 8-29 on page 169	0x2E/0x2F	0x00
Get Serial Interface Properties Table 8-30 on page 172	0x2E/0x2F	0x01
Set Serial Interface Properties Table 8-31 on page 173	0x2E/0x2F	0x02
Get Debug Level Table 8-32 on page 174	0x2E/0x2F	0x03
Set Debug Level Table 8-33 on page 175	0x2E/0x2F	0x04
Get Hardware Address Table 8-34 on page 176	0x2E/0x2F	0x05
Set Hardware Address Table 8-35 on page 176	0x2E/0x2F	0x06
Get Handle Switch Table 8-36 on page 177	0x2E/0x2F	0x07
Set Handle Switch Table 8-37 on page 178	0x2E/0x2F	0x08
Get Payload Communication Time-Out Table 8-38 on page 178	0x2E/0x2F	0x09
Set Payload Communication Time-Out Table 8-39 on page 179	0x2E/0x2F	0x0A
Enable Payload Control Table 8-40 on page 180	0x2E/0x2F	0x0B
Disable Payload Control Table 8-41 on page 180	0x2E/0x2F	0x0C
Reset IPMC Table 8-42 on page 181	0x2E/0x2F	0x0D
Hang IPMC Table 8-43 on page 181	0x2E/0x2F	0x0E
Graceful Reset Table 8-44 on page 182	0x2E/0x2F	0x11
Get Payload Shutdown Time-Out Table 8-45 on page 183	0x2E/0x2F	0x15
Set Payload Shutdown Time-Out Table 8-46 on page 184	0x2E/0x2F	0x16
Get Module State Table 8-47 on page 184	0x2E/0x2F	0x27
Enable Module Site Table 8-48 on page 186	0x2E/0x2F	0x28
Disable Module Site Table 8-49 on page 186	0x2E/0x2F	0x29

Table 8-27 Pigeon Point Extension Commands (continued)

Command	NetFn (Request/Response)	CMD
Reset Carrier SDR repository Table 8-50 on page 187	0x2E/0x2F	0x33

Some of the following commands refer to IPMC modes which are defined as follows:

Table 8-28 IPMC Modes

Mode	Description
Standalone	In standalone mode, the carrier IPMC disconnects from IPMB-0 but keeps on listening to the serial debug and payload interfaces and serving requests coming from them, as well as managing the modules, AMC point-to-point (P2P) and clock E-keying. Standalone mode is intended for debugging purposes and/or operation in a non-ATCA environment. In standalone mode, the carrier IPMC automatically activates and deactivates the on-carrier payload and modules whenever it does not violate any carrier limitations.
Manual standalone	Manual standalone mode is equivalent to standalone mode with only one exception: carrier IPMC control over the on-carrier payload is automatically disabled in manual standalone mode.

8.4.1 Get Status Command

The Get Status command can be used by the payload software to retrieve the status of the IPMC.

Table 8-29 Get Status Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

Table 8-29 Get Status Command Description (continued)

Type	Byte	Data Field
	5	Bit [7] Graceful Reboot Request If set to "1", indicates that the payload is requested to initiate the graceful reboot sequence. Bit [6] Diagnostic Interrupt Request If set to "1", indicates that a payload diagnostic interrupt request has arrived. Bit [5] Shutdown Alert If set to "1", indicates that the payload is going to be shutdown. Bit [4] Reset Alert If set to "1", indicates that the payload is going to be reset. Bit [3] Sensor Alert If set to "1", indicates that at least one of the IPMC sensors detects a threshold crossing. Bits [2:1] Mode The current IPMC modes are defined as: 0: Normal 1: Standalone, for a description refer to Table 8-28 2: Manual Standalone, for a description refer to Table 8-28 Bit [0] Control If set to 0, the IPMC control over the payload is disabled.
	6	Bits [4:7] Metallic Bus 2 Events These bits indicate pending Metallic Bus 2 requests arrived from the shelf manager: 0: Metallic Bus 2 Query 1: Metallic Bus 2 Release 2: Metallic Bus 2 Force 3: Metallic Bus 2 Free Bits [0:3] Metallic Bus 1 Events These bits indicate pending Metallic Bus 1 requests arrived from the shelf manager: 0: Metallic Bus 1 Query 1: Metallic Bus 1 Release 2: Metallic Bus 1 Force 3: Metallic Bus 1 Free

Table 8-29 Get Status Command Description (continued)

Type	Byte	Data Field
	7	Bits [4:7] Clock Bus 2 Events These bits indicate pending Clock Bus 2 requests arrived from the shelf manager: 0: Clock Bus 2 Query 1: Clock Bus 2 Release 2: Clock Bus 2 Force 3: Clock Bus 2 Free Bits [0:3] Clock Bus 1 Events These bits indicate pending Clock Bus 1 requests arrived from the shelf manager: 0: Clock Bus 1 Query 1: Clock Bus 1 Release 2: Clock Bus 1 Force 3: Clock Bus 1 Free
	8	Bits [4:7] Reserved Bits [0:3] Clock Bus 3 Events These bits indicate pending Clock Bus 3 requests arrived from the shelf manager: 0: Clock Bus 3 Query 1: Clock Bus 3 Release 2: Clock Bus 3 Force 3: Clock Bus 3 Free

8.4.2 Get Serial Interface Properties Command

The Get Serial Interface Properties command is used to get the properties of a particular serial interface.

Table 8-30 Get Serial Interface Properties Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Interface ID 0: Serial Debug Interface
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Bit [7] Echo On If this bit is set, the IPMC enables echo for the given serial interface. Bits [6:4] Reserved Bits [3:0] Baud Rate ID The baud rate ID defines the interface baud rate as follows: 0: 9600 bps 1: 19200 bps 2: 38400 bps 3: 57600 bps (unsupported) 4: 115200 bps (unsupported)

8.4.3 Set Serial Interface Properties Command

The Set Serial Interface Properties command is used to set the properties of a particular serial interface.

Table 8-31 Set Serial Interface Properties Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Interface ID 0: Serial Debug Interface
	5	Bit [7] Echo On If this bit is set, the IPMC enables echo for the given serial interface. Bits [6:4] Reserved Bits [3:0] Baud Rate ID The baud rate ID defines the interface baud rate as follows: 0: 9600 bps 1: 19200 bps 2: 38400 bps 3: 57600 bps (unsupported) 4: 115200 bps (unsupported)
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.4 Get Debug Level Command

The Get Debug Level command gets the current debug level of the IPMC firmware.

Table 8-32 Get Debug Level Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Bit [7] IPMB-L Dump Enable If set to 1, the IPMC provides a trace of IPMB-L messages that are arriving to/going from the IPMC via IPMB-L. Bit [6] n/a Bit [5] KCS Dump Enable If set to "1", the IPMC provides a trace of KCS messages that are arriving to/going from the IPMC via KCS. Bit [4] IPMB Dump Enable If set to "1", the IPMC provides a trace of IPMB messages that are arriving to/going from the IPMC via IPMB-O. Bit [3] n/a Bit [2] Alert Logging Enable If set to "1", the IPMC outputs important alert messages onto the serial debug interface. Bit [1] Low-level Error Logging Enable If set to "1", the IPMC outputs low-level error/diagnostic messages onto the serial debug interface. Bit [0] Error Logging Enable If set to "1", the IPMC outputs error/diagnostic messages onto the serial debug interface.

8.4.5 Set Debug Level Command

The Set Debug Level command sets the current debug level of the IPMC firmware.

Table 8-33 Set Debug Level Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Bit [7] IPMB-L Dump Enable If set to "1", the IPMC provides a trace of IPMB-L messages that are arriving to/going from the IPMC via IPMB-L. Bit [6] n/a Bit [5] KCS Dump Enable If set to "1", the IPMC provides a trace of KCS messages that are arriving to/going from the IPMC via KCS. Bit [4] IPMB Dump Enable If set to "1", the IPMC provides a trace of IPMB messages that are arriving to/going from the IPMC via IPMB-O. Bit [3] n/a Bit [2] Alert Logging Enable If set to "1", the IPMC outputs important alert messages onto the serial debug interface. Bit [1] Low-level Error Logging Enable If set to "1", the IPMC outputs low-level error/diagnostic messages onto the serial debug interface. Bit [0] Error Logging Enable If set to "1", the IPMC outputs error/diagnostic messages onto the serial debug interface.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.6 Get Hardware Address Command

The Get Hardware Address command reads the hardware address of the IPMC.

Table 8-34 Get Hardware Address Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Hardware Address

8.4.7 Set Hardware Address Command

The Set Hardware Address command allows the user to override the hardware address read from the hardware when the IPMC operates in (manual) standalone mode (for a description refer to Table 8-28).

Table 8-35 Set Hardware Address Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Hardware Address If set to 00, the ability to override the hardware address is disabled. NOTE: A hardware address change only takes effect after an IPMC reset.
Response Data	1	Completion Code

Table 8-35 Set Hardware Address Command Description (continued)

Type	Byte	Data Field
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.8 Get Handle Switch Command

The Get Handle Switch command reads the state of the hot-swap handle of the IPMC. Overriding of the handle switch state is allowed only if the IPMC operates in (manual) standalone mode (for a description refer to Table 8-28).

Table 8-36 Get Handle Switch Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	FRU ID (specify as 0)
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Handle Switch Status 0x00: The handle switch is open. 0x01: The handle switch is closed. 0x02: The handle switch state is read from hardware.

8.4.9 Set Handle Switch Command

The Set Handle Switch command sets the state of the hot-swap handle switch in (manual) standalone mode (for a description refer to Table 8-28).

Table 8-37 Set Handle Switch Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	FRU ID (specify as 0)
	5	Handle Switch Status 0x00: The handle switch is open. 0x01: The handle switch is closed. 0x02: The handle switch state is read from hardware.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.10 Get Payload Communication Time-Out Command

The Get Payload Communication Time-Out command reads the payload communication time-out value.

Table 8-38 Get Payload Communication Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code

Table 8-38 Get Payload Communication Time-Out Command Description (continued)

Type	Byte	Data Field
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Payload Time-out Payload communication time-out measured in hundreds of milliseconds. Thus, the payload communication time-out may vary from 0.1 to 25.5 seconds.

8.4.11 Set Payload Communication Time-Out Command

The Set Payload Communication Time-Out command sets the payload communication time-out value.

Table 8-39 Set Payload Communication Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Payload Time-out Payload communication time-out measured in hundreds of milliseconds. Thus, the payload communication time-out may vary from 0.1 to 25.5 seconds.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.12 Enable Payload Control Command

The Enable Payload Control command enables payload control from the serial debug interface.

Table 8-40 Enable Payload Control Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.13 Disable Payload Control Command

The Disable Payload Control command disables payload control from the serial debug interface.

Table 8-41 Disable Payload Control Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.14 Reset IPMC Command

The Reset IPMC command allows the payload to reset the IPMC over the KCS host interface.

Table 8-42 Reset IPMC Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Reset Type Code 0x00: Cold IPMC reset to the current mode 0x01: Cold IPMC reset to the Normal mode 0x02: Cold IPMC reset to the Standalone mode, for a description refer to Table 8-28 0x03: Cold IPMC reset to the Manual Standalone mode, for a description refer to Table 8-28 0x04: Reset the IPMC and enter Upgrade mode
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.15 Hang IPMC Command

The IPMC provides a way to test the watchdog timer support by implementing the Hang IPMC command, which simulates firmware hanging by entering an endless loop.

Table 8-43 Hang IPMC Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code

Table 8-43 Hang IPMC Command Description (continued)

Type	Byte	Data Field
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.16 Graceful Reset Command

The IPMC supports the Graceful Reboot option of the FRU Control command. On receiving such a command, the IPMC sets the Graceful Reboot Request bit of the IPMC status, sends a status update notification to the payload, and waits for the Graceful Reset command from the payload. If the IPMC receives such a command before the payload communication time-out time, it sends the 0x00 completion code (Success) to the shelf manager. Otherwise, the 0xCC completion code is sent.

The IPMC does not reset the payload upon receiving the Graceful Reset command or time-out. If the IPMC participation is necessary, the payload must request the IPMC to perform a payload reset. The Graceful Reset command is also used to notify the IPMC about the completion of the payload shutdown sequence.

Table 8-44 Graceful Reset Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.17 Get Payload Shutdown Time-Out Command

When the shelf manager commands the IPMC to shut down the payload (i.e. sends the Activate FRU (Deactivate) command), the IPMC notifies the payload by forwarding the command Activate FRU (Deactivate) to the KCS interface. Provided the OpenIPMI driver has registered this command for notification, the payload gets notified. Upon receiving this notification, the payload software is expected to initiate the payload shutdown sequence. After performing this sequence, the payload should send the Graceful Reset command to the IPMC over the payload Interface to notify the IPMC that the payload shutdown is complete.

To avoid deadlocks that may occur if the payload software does not respond, the IPMC provides a special time-out for the payload shutdown sequence. If the payload does not send the Graceful Reset command within a definite period of time, the IPMC assumes that the payload shutdown sequence is finished, and resets the payload.

Table 8-45 Get Payload Shutdown Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5:6	Time-Out measured in hundreds of milliseconds, LSB first

8.4.18 Set Payload Shutdown Time-Out Command

The Set Payload Shutdown Time-Out command is defined as follows.

Table 8-46 Set Payload Shutdown Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4:5	Time-Out measured in hundreds of milliseconds, LSB first
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.19 Get Module State Command

The Get Module State command is used to query the state of a module (RTM with site ID1) using any of the external interfaces.

Table 8-47 Get Module State Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

Table 8-47 Get Module State Command Description (continued)

Type	Byte	Data Field
	5	Module Status Bit [0] 0: Module site is enabled. 1: Module site is disabled. Bit [1] 0: Module is not present. 1: Module is present. Bit [2] 0: Management power is disabled. 1: Management power is enabled. Bit [3] 0: Management power is bad. 1: Management power is good. Bit [4] 0: Payload power is disabled. 1: Payload power is enabled. Bit [5] 0: Payload power is bad. 1: Payload power is good. Bit [6] 0: IPMB-L buffer is not attached. 1: IPMB-L buffer is attached. Bit [7] 0: IPMB-L buffer is not ready. 1: IPMB-L buffer is ready.

8.4.20 Enable Module Site Command

The Enable Module Site command is used to enable a module site.

Table 8-48 Enable Module Site Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00

8.4.21 Disable Module Site Command

The Disable Module Site command is used to disable a module site. If a module site is disabled, the IPMC firmware ignores the module inserted and acts as if the module is not present.

Table 8-49 Disable Module Site Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.22 Reset Carrier SDR Repository Command

The Reset Carrier SDR Repository command is used to clear and rebuild the carrier SDR repository.

Table 8-50 Reset Carrier SDR Repository Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

9.1 FRU Information

The blade provides the following FRU information in FRU ID 0.

Table 9-1 FRU information

Area	Description	Value	Access
Internal use area	Not used		
Board info area	Mfg date / time	According to Platform Management FRU information Storage Definition v1.0	r
	Board manufacturer	'EMERSON'	r
	Board product name	Product name of the specific blade variant	r
	Board serial number	Defined by Artesyn	r
	Board part number	Defined by Artesyn	r
Product info area	Product manufacturer	'EMERSON'	r
	Product name	Product name of the specific blade variant	r
	Product serial number	Defined by Artesyn	r
	Product part number	Defined by Artesyn	r

Table 9-1 FRU information (continued)

Area	Description	Value	Access
Multi record info area	Blade Point-To-Point Connectivity Record Area	PICMG record ID 0x14. The contents are described in the section 'E- Keying'.	r
	Carrier Information table record	PICMG record ID 0x1A.	r
	Carrier activation and current management record	PICMG record ID 0x17.	r
	Carrier point-to-point connectivity records	PICMG record ID 0x18.	r
	AMC point-to-point connectivity	PICMG record ID 0x19.	r
	User Info Area	Artesyn OEM ID: 0x48, 0x0E, 0x00, 0x00 Followed by 255 byte of user info area data	r/w
	Custom usage	Min. 256 Byte available	r/w

Table 9-2 MAC Address Location

MAC Address records	Location	Comments
1	Base interface 1	
2	Base interface 2	
3	Fabric interface 1	
4	Fabric interface 2	
5	Update channel	
6	Front panel	

Table 9-2 MAC Address Location (continued)

MAC Address records	Location	Comments
7	Connect to AMC Port 0 or 10	Only valid for variants with AMC bay populated
8	Connect to AMC Port 1 or 11	
9	Connect to AMC Port 8	
10	Connect to AMC Port 9	

9.2 MAC Address Record

The blade provides one OEM FRU record which contains information about on-board MAC addresses.

The format of the record is described in the following table.

Table 9-3 Artesyn MAC Addresses Record

Offset	Length	Description
0	1	Record Type ID. A value of C0h (OEM) shall be used for Artesyn OEM records.
1	1	End of List / Version [7] End of List. Set to 1b for the last record [6:4] Reserved. Write as 000b. [3:0] Record format version. Write as 2h.
2	1	Record Length
3	1	Record Checksum (zero checksum)
4	1	Header Checksum (zero checksum)
5	1	LSB of Manufacturer ID. Write as CDh.
6	1	Second Byte of Manufacturer ID. Write as 65h.
7	1	MSB of Manufacturer ID. Write as 00h.
8	1	Artesyn Record ID. 01h for Artesyn MAC Address Record.
9	1	Record Format Version. 00h for this specification.

Table 9-3 Artesyn MAC Addresses Record (continued)

Offset	Length	Description
10	1	Number of MAC Address Descriptors (N).
11	N*7	Artesyn MAC Address Descriptors. Refer to Table 21 for definitions of Artesyn MAC Address Descriptor.

Table 9-4 Artesyn MAC Address Descriptor

Offset	Length	Description
0	1	Interface Type. Refer to the table below for Interface Type Assignments.
1	6	MAC Address. First Octet comes first.

Table 9-5 Interface Type Assignments

Interface Type	Description
01h	ATCA Base Interface or AMC / MicroTCA Common Options Region
02h	ATCA Fabric Interface or AMC / MicroTCA Fat Pipe Region
03h	Front Panel
04h	AMC / MicroTCA Extended Fat Pipe Region

9.3 E-Keying

The following table lists the e-keying information provided by the blade. The respective information is contained in the point-to-point connectivity record area.

The fibre channel interfaces (link type extension 2) described in the point-to-point connectivity record area are physically not supported by the blade.

Table 9-6 Contents of the Blade Point-to-Point Connectivity Record Area

No.	Link Grouping ID	Interface	Channel Number	Ports	Link Type	Link Type Extension	Link Descriptor Value
1	0	0 (Base Interface)	1	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0x01	0	
2	0	0 (Base Interface)	2	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0x01	1	
3	0	1 (Fabric Interface)	1	0 -SET 1 - SET 2 -SET 3 -SET	0x02	1	
4	0	1 (Fabric Interface)	1	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0x02	0	
5	0	1 (Fabric Interface)	2	0 -SET 1 - SET 2 -SET 3 -SET	0x02	1	
6	0	1 (Fabric Interface)	2	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0x02	0	
7	0	2 (Update Channel Interface)	1	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0xF0	0	

Table 9-6 Contents of the Blade Point-to-Point Connectivity Record Area (continued)

No.	Link Grouping ID	Interface	Channel Number	Ports	Link Type	Link Type Extension	Link Descriptor Value
8	0	2 (Update Channel Interface)	2	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0xF1	0	
9	0	2 (Update Channel Interface)	2	0 - NOT SET 1 - SET 2 - NOT SET 3 - NOT SET	0xF2	0	
10	0	2 (Update Channel Interface)	2	0 - NOT SET 1 - NOT SET 2 - SET 3 - NOT SET	0xF3	0	
11	0	2 (Update Channel Interface)	2	0 - NOT SET 1 - NOT SET 2 - NOT SET 3 - SET	0xF4	0	

9.4 Power Configuration

Table 9-7 Power Configuration

Item	Value	Description
Dynamic power reconfiguration support	No	While the blade is powered, it supports only one power level.
Dynamic power configuration	No	The power level is fixed and does not change).
Number of power draw levels	2	The amount of possible power levels
Early Power Draw Levels, Watt	-	Complete early power level including IPMC
Steady state Power Draw Levels, Watt	Power level 1: 116 W Power level 2: 152 W	Complete steady power consumption including IPMC
Transition from early to steady levels, sec	0s	-

9.5 Sensor Data Records

The sensors available on the blades are shown in the table below.

Table 9-8 IPMI Sensors Overview

Sensor Name	Sensor Type	Sensor Number
Hotswap Carrier	PICMG 3.0:FRU HotSwap	0x00
Hotswap_AMC	PICMG 3.0:FRU HotSwap	0x01
Hotswap_RTM	PICMG 3.0:FRU HotSwap	0x02
-48V A Volts	Voltage	0x03
-48V B Volts	Voltage	0x04
-48V Amps	Current	0x05
HoldUP Cap Volts	Voltage	0x06

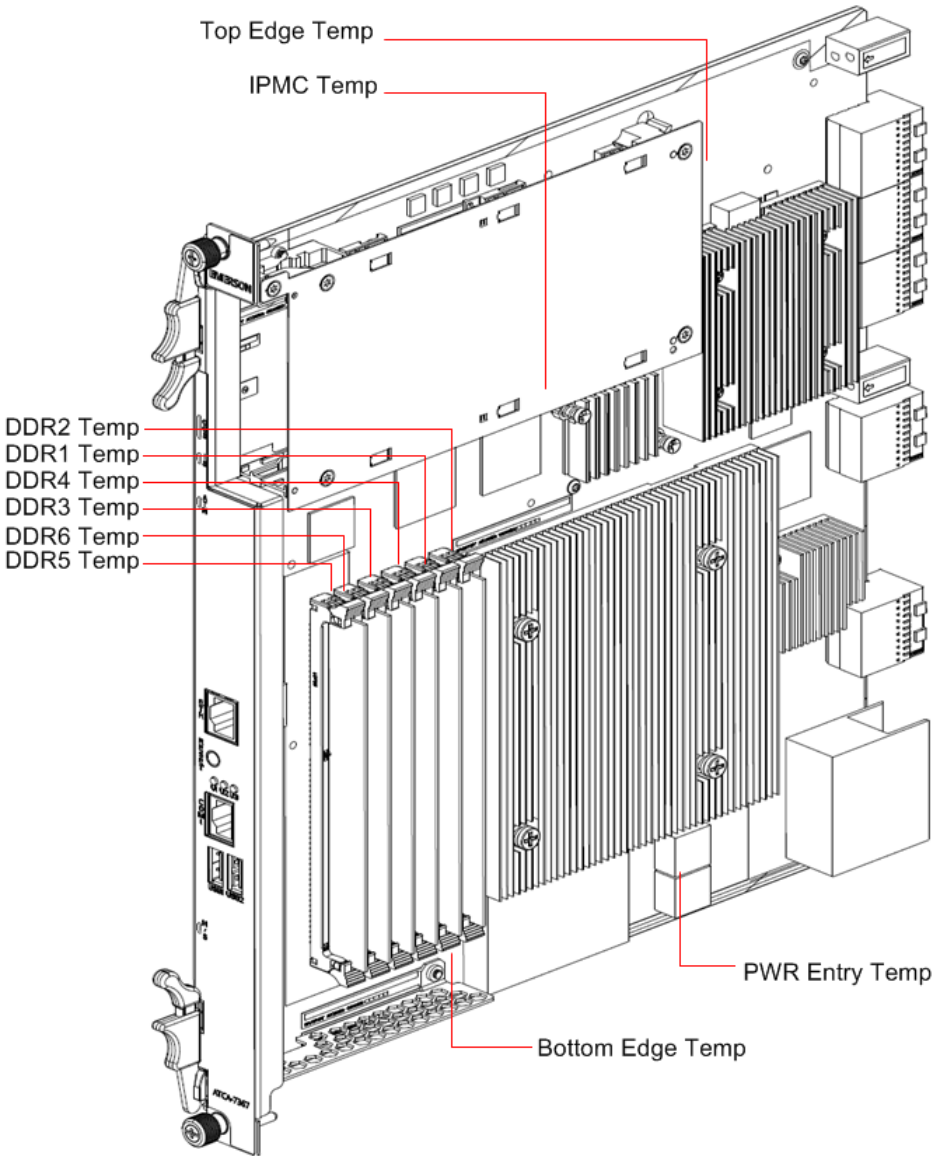
Table 9-8 IPMI Sensors Overview (continued)

Sensor Name	Sensor Type	Sensor Number
PWR Entry Temp	Temperature	0x07
PWR Enrty Status	Power Entry Module Status	0x08
Bottom Edge Temp	Temperature	0x09
Top Edge Temp	Temperature	0x0A
IPMC Temp	Temperature	0x0B
CPU Temp	Temperature	0x0C
DDR 1 Temp	Temperature	0x0D
DDR 2 Temp	Temperature	0x0E
DDR 3 Temp	Temperature	0x0F
DDR 4 Temp	Temperature	0x10
DDR 5 Temp	Temperature	0x11
DDR 6 Temp	Temperature	0x12
IPMB Physical	PICMG 3.0:IPMB Physical Link	0x13
BMC Watchdog	Watchdog 2	0x14
IPMC POST	Management Subsystem Health	0x15
Version Change	Version Change	0x16
Fw Progress	System Firmware Progres	0x17
OS Boot	OS boot	0x18
Boot Error	Boot Error	0x19
Boot Initiated	System Boot Initiated	0x1A
POST Code	Artesyn-specific Discrete Digital	0x1B
ATCA-7367 IPMC	Artesyn IPMC Status	0x1C
Power Good	Entity Presence	0x1D
Boot Bank	Artesyn-specific Discrete Digital	0x1E
Reset Source	Artesyn-specific Discrete Digital	0x1F
CPU Status	Processor	0x20

Hotswap_AMC(0x01) sensor only exists for variants with the AMC bay populated. The total number of sensors if there is no AMC in the slot is 0x20.

The following figure shows the locations of all temperature sensors available on-board.

Figure 9-1 Location of Temperature Sensors



The sensors available on the blades are detailed in the table below.

For sensor threshold definition please use the "ipmitool" available at http://sourceforge.net/projects/ipmitool/files/ipmitool/ with the parameter "sensor".

Table 9-9 Sensor Data Records

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x00	Hot Swap Carrier	Hot Swap 0xF0	Sensor-specific discrete 0x6F	[7:4] = See IPMC Spec [3:0] = Current State (0, 1, 2, 3, 4, 5, 6 or 7)	[7:4] = Cause [3:0] = Previous State	[7:0] =FRU ID	For the Field: Current State/Previous State 0x0: M0 0x1: M1 0x2: M2 0x3: M3 0x4: M4 0x5: M5 0x6: M6 0x7: M7	Asrt	Auto
0x01	Hotswap_AMC	Hot Swap 0xF0	Sensor-specific discrete 0x6F	[7:4] = See IPMC Spec [3:0] = Current State (0, 1, 2, 3, 4, 5, 6 or 7)	[7:4] = Cause [3:0] = Previous State	[7:0] =FRU ID	For the Field: Current State/Previous State 0x0: M0 0x1: M1 0x2: M2 0x3: M3 0x4: M4 0x5: M5 0x6: M6 0x7: M7	Asrt	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 9-9 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x02	Hotswap_RTM	Hot Swap 0xF0	Sensor-specific discrete 0x6F	[7:4] = See IPMC Spec [3:0] = Current State (0, 1, 2, 3, 4, 5, 6 or 7)	[7:4] = Cause [3:0] = Previous State	[7:0] = FRU ID	For the Field: Current State/Previous State 0x0: M0 0x1: M1 0x2: M2 0x3: M3 0x4: M4 0x5: M5 0x6: M6 0x7: M7	Asrt	Auto
0x03	-48V A Volts	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
0x04	-48V B Volts	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt/Deass	Auto
0x05	-48V Amps	Current 0x03	Threshold 0x01				No event for this sensor		Auto
0x06	HoldUp Cap Volts	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt/Deass	Auto
0x07	PWR Entry Temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	uc nc	Asrt / Deass	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 9-9 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x08	PWR Entry Status	OEM 0xD7	Sensor-specific discrete 0x6F	[7:4] = (See IPMC Spec) [3:0] = 0h	Synchor Pwr Entr Module: [6] = VOUT_low [5] = Hotswap [4] = Holdup [2] = Alarm [1] = Enable_B [0] Enable_A Emerson Pwr Entry Module: [7] = DIG_Fault [6] = HUCapEngage [5] = Hotswap_Enable [4] = HUCap_Switch [3] = Alarm_Control [1] = DIG_Alarm [0] = Sec_MCU_Fault All other bits are reserved	[7:6] = Pwr Entry Module 0 = Synchor 1 = Emerson Emerson Pwr Entry Module: [2] = DIG_EnableA [1] = DIG_EnableB [0] = Mcu_Fault All other bits are reserved	Pwr Entry Module Status Change detected	Asrt	Auto
0x09	Bottom Edge Temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x0A	Top Edge Temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x0B	IPMC temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x0C	CPU temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x0D	DDR 1 temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x0E	DDR 2 temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x0F	DDR 3 temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 9-9 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x10	DDR 4 temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x11	DDR 5 temp	Temp 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x12	DDR 6 temp	Temp 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x13	IPMB Physical	Physical IPMB-0 0xF1	Sensor-specific discrete 0x6F	[7:4] = See IPMC Spec [3:0] = Offset (0, 1, 2 or 3)	[7:4] = Channel Number. For the ATCA-7367, this is 0h to indicate IPMB-0 [3:0] = Reserved	reading	0x0: IPMB-A disabled, IPMB-B disabled 0x1: IPMB-A enabled, IPMB-B disabled 0x2: IPMB-A disabled, IPMB-B enabled 0x3: IPMB-A enabled, IPMB-B enabled	Asrt	Auto
0x14	BMC Watchdog	Watchdog 2 0x23	Sensor-specific discrete 0x6F	[7:4] = See IPMC Spec [3:0] = Offset (0, 1, 2, 3 or 8)	See IPMI specifications	0xFF	0x0: Timer expired 0x1: Hard Reset 0x2: Power Down 0x3: Power Cycle 0x8: Timer Interrupt	Asrt	Auto
0x15	IPMC POST	Management Subsystem Health 0x28	Sensor-specific discrete 0x06	[7:4] = (See IPMC Spec) [3:0] = Offset (0, 1)	0xFF	0xFF	0x0: Performance Met 0x1: Performance Lags	Asrt	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 9-9 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x16	Version change	Version Change 0x2B	Sensor-specific discrete 0x6F	[7:4] = (See IPMC Spec) [3:0] = Offset (0, 1, 2, 3, 4, 5, 6, 7)	Change type	0xFF	0x0: Hardware change 0x1: Firmware or software change 0x2: Hardware incompatibility 0x3: Firmware or software incompatibility 0x4: Entity is of an invalid hardware version 0x5: Entity contains invalid F/W,software 0x6: Hardware Change successful 0x7: Software or F/W change successful	Asrt	Auto
0x17	Fw Progress	System Firmware Progress 0x0F	Sensor-specific discrete 0x6F	[7:4] = (See IPMC Spec) [3:0] = Offset (0, 1, 2)	See IPMI Spec	See IPMI Spec	0x0: System Firmware Error 0x1: System Firmware Hang 0x2: System Firmware Progress	Asrt	Auto
0x16	OS Boot	OS Boot 0x1F	Sensor-specific discrete 0x6F	[7:4] = (See IPMC Spec) [3:0] = Offset (0, 1, 2, 3, 4, 5, 6)	0xFF	0xFF	0x0: A: boot completed 0x1: C: boot completed 0x2: PXE boot completed 0x3: Diagnostic boot completed 0x4: CD_ROM boot completed 0x5: ROM boot completed 0x6: boot completed	Asrt	Auto
0x19	Boot Error	Boot Error 0x1E	Sensor-specific discrete 0x6F	[7:4] = (See IPMC Spec) [3:0] = Offset (0, 1, 2, 3, 4)	0xFF	0xFF	Reserved for future use.	Asrt	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 9-9 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x1A	Boot Initiated	System Boot Initiated 0x1D	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4	Event Data Byte 2 [7:4] Active BIOS major version [3:0] Active BIOS minor version	Event Data Byte 3 [7:4] Active BIOS sub-minor version [3:0] Reserved	0x0: Initiated by power up 0x1: Initiated by hard reset 0x2: Initiated by warm reset 0x3: User requested PXE boot 0x4: Automatic boot to diagnostic	Asrt	Auto
0x1B	POST code	OEM 0xD2	Sensor-specific discrete 0x6F	-	-	-	0x0: No events for this sensor. Reading according to EFI BIOS port80 status codes.	-	Auto
0x1C	ATCA-7367 IPMC	OEM 0xD5	Sensor-specific discrete 0x6F	-	-	-	No event for this sensor Reading Value: [0:2] Reset Cause 0x1: Watchdog Reset 0x2: Software Reset 0x4: Power on Reset [3]: Reserved [4:6] Reset Type 0x1: Hard Boot 0x2: Cold Boot 0x4: Warm Boot [7]: Reserved	-	Auto
0x1D	Power Good	Entity Presence 0x25	Sensor-specific discrete 0x6F	[7:4] = See IPMC Spec [3:0] = Offset (0, 1)	0xFF	0xFF	0x0: Entity Present 0x1: Entity Absent	Asrt	Auto
0x1E	Boot Bank	OEM 0xD2	Sensor-specific discrete 0x6F	0x0	0xFF	0xFF	Sending this event when Payload CPU boot bank changed	Asrt	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 9-9 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x1F	Reset Source	OEM 0xD2	Sensor-specific discrete 0x6F	0xA0	bit0: RST_N: Payload Power-on reset bit1: Reserved bit2: FRB_PB_RST_N: Front board power button reset bit3: PLD_PL_RST_N: Payload Reset from PLD (IPMC) bit4: RTM_PB_RST_N: RTM power button reset bit5: WDG_RST_N: FPGA internal watchdog reset bit6: BIOS_RST_N: BIOS reset payload request bit7: OSYS_RST_N: OS reset payload 0: Reset not occurred 1: Reset occurred	[7:2] = Reserved [1] = IPMC Watchdog Timeout 0: No IPMC Watchdog Timeout 1: IPMC Watchdog Timeout occurred [0] = IPMC Watchdog Pre-Timeout 0: No IPMC Watchdog Pre-Timeout 1: IPMC Watchdog Pre-Timeout occurred	0x0: Payload Reset detected. Cause delivered in Event Byte 2/3	Asrt	Auto
0x20	CPU Status	Processor 0x07	Sensor-specific discrete 0x6F	[7:4] = See IPMC Spec [3:0] = Offset (1)	0xFF	0xFF	0x1: Thermal Trip	Asrt	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

10.1 HPM.1 Firmware Upgrade

10.1.1 Overview

The primary update mechanism for the ATCA-7367 blades is the FCU tool which is delivered with the BBS package for the board. However, the ATCA-736X board family also supports upgrade of the firmware with the HPM.1 specification. Upgradable components of the board include the BIOS flash, FPGA flash, and IPMC flash. For update, it is recommended to use the Pigeon Point System modified Ipmitool.

10.1.2 Installing the Ipmitool

procedure

1. Get the Pigeon Point System Ipmitool from the package (Ipmitool-1.8.9-pps-8.tgz).
2. Extract the source code.

   ```
   Prompt>tar -xzvf Ipmitool-1.8.9-pps-<version>.tgz
   ```

3. Go to the directory where you have extracted the Ipmitool.

   ```
   Prompt>cd <path>/Ipmitool-1.8.9-pps-<version>
   ```

4. Build the Ipmitool.
   ```
   Prompt>./configure && make && make install
   ```

10.1.2.1 Update Procedure

The Ipmitool HPM update requires two steps for an update:

1. Upgrade the component.
   Example: **`ipmitool hpm upgrade <file>`**
2. Activate the component.
   Example: **`ipmitool hpm activate`**

Both steps can also be integrated into one command.

```
ipmitool hpm upgrade <file> activate
```

10.1.3 Interface

The HPM.1 upgrade supports three different interfaces for upgrading the firmware. These are KCS, IPMB-0, and LAN over BASE. The LAN interface is only supported if the payload is powered on (M4). The BASE Ethernet controller also has to be powered on for this feature.

10.1.3.1 KCS Interface

The standard way to upgrade the firmware of the payload is through the KCS interface. Update through this interface is the fastest HPM.1 upgrade. The images and the Ipmi tool need to be on the payload to be upgraded.

Example:

```
Prompt>ipmitool hpm upgrade <file>
```

10.1.3.2 IPMB-0

This interface represents the backplane IPMI bus and allows remote firmware upgrade. The count of the simultaneous upgrades is limited because of the bus speed.

Example from shelf manger:

```
Prompt>ipmitool -t 0x92 hpm upgrade <file>
```

Example with RMCP+:

```
Prompt>ipmitool -I lan -H 192.168.34.8 -U Administrator -P
Administrator -t 0x92 hpm upgrade <file>
```

10.1.3.3 IPMI over LAN (BASE)

The IPMI over LAN interface uses the BASE Ethernet controller to do firmware upgrades. The interface has to be configured before the first use. Configuring this interface is described in Chapter 7, *Configuring SOL Parameters, on page 140*.

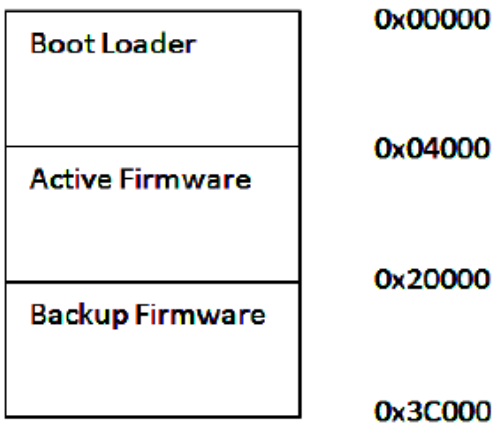
Example:

```
Prompt>Ipmitool -I lan -H 172.16.0.221 -U "" -P "" hpm upgrade
<file>
```

10.2 IPMC Upgrade

The IPMC component is fully HPM.1 compatible and contains three elements as shown on the figure below.

Figure 10-1 IPMC Component Elements



There are images for the boot loader and the firmware. There is also a combined image containing the boot loader and the firmware. The Boot loader update should only be done if it's required.

The boot loader does not perform any upgrade action. The boot loader is able to boot either of two redundant copies of the firmware in the flash depending on the current value of the special partition status byte that is stored in the internal IPMC EEPROM. The boot loader can fall back to the backup copy by booting the alternate partition. The boot loader manages two firmware partitions; the active and backup partition. It is responsible for detecting if the active firmware

is invalid or has failed. If the active firmware failed or is invalid, the Boot loader will switch to the backup partition. When switching, the partitions change their roles. Switching of the partitions also takes place when the firmware is upgraded and activated using the HPM.1 upgrade procedure.

The firmware image is the regular firmware and change with every update.

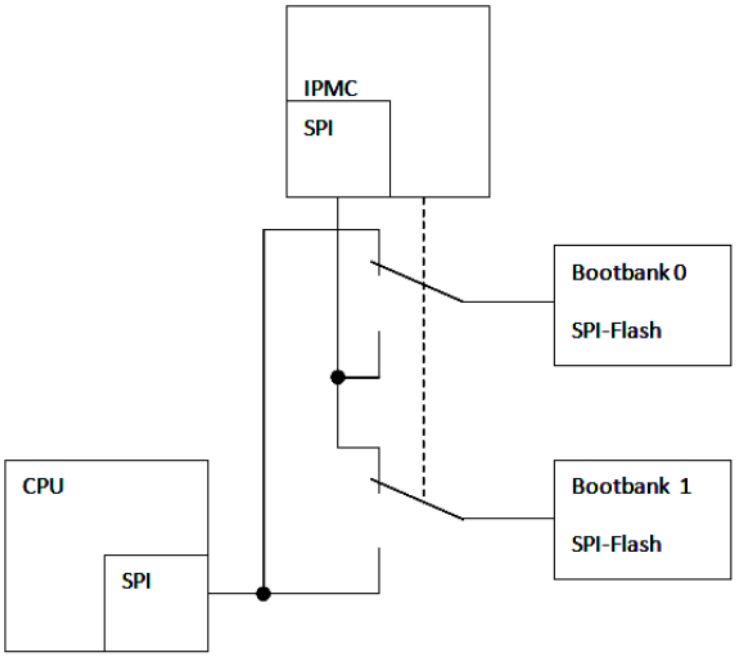
10.3 BIOS/FPGA Upgrade

BIOS has two independent boot banks. The FPGA has a single boot bank. The switching of this boot banks is not supported by HPM commands of ATCA-736X.

Both BIOS/FPGA boot banks can be updated with HPM.1. The BIOS/FPGA upgrade is not fully HPM.1 compatible due to the fact that payload update of this device must also be possible. This leads to the fact that an automatic boot bank switching via the IPMC is not possible which is a requirement for HPM.1 to activate.

Payload always has access to the active BIOS boot bank and the IPMC always has access to the inactive BIOS boot bank. Users must not upgrade the FPGA firmware during payload power up phase through the IPMC because there is only one FPGA flash on this platform. All HPM.1 commands are directed to the inactive BIOS boot bank (this includes "get component properties"). The following figure shows the connection of the SPI busses which are switched with "Set System Boot Options" -> Boot Bank (parameter 0x96). Description can be found in the document "OEM Extensions for ATCA / MicroTCA Hardware Platform Management System". HPM activate command is not supported for the BIOS/FPGA component.

Figure 10-2 SPI Busses Connection



FPGA and BIOS upgrade may last from fifteen minutes up to two hours. The time varies with the selected programming interface. A power cycle is required after the BIOS/FPGA update.

10.4 Upgrade Package

The HPM upgrade package for this release contains the following files:

Table 10-1 HPM Upgrade Package

Filename	Description
atca-7367-ipmc-boot.hpm	HPM file contains only the boot loader image

Table 10-1 HPM Upgrade Package (continued)

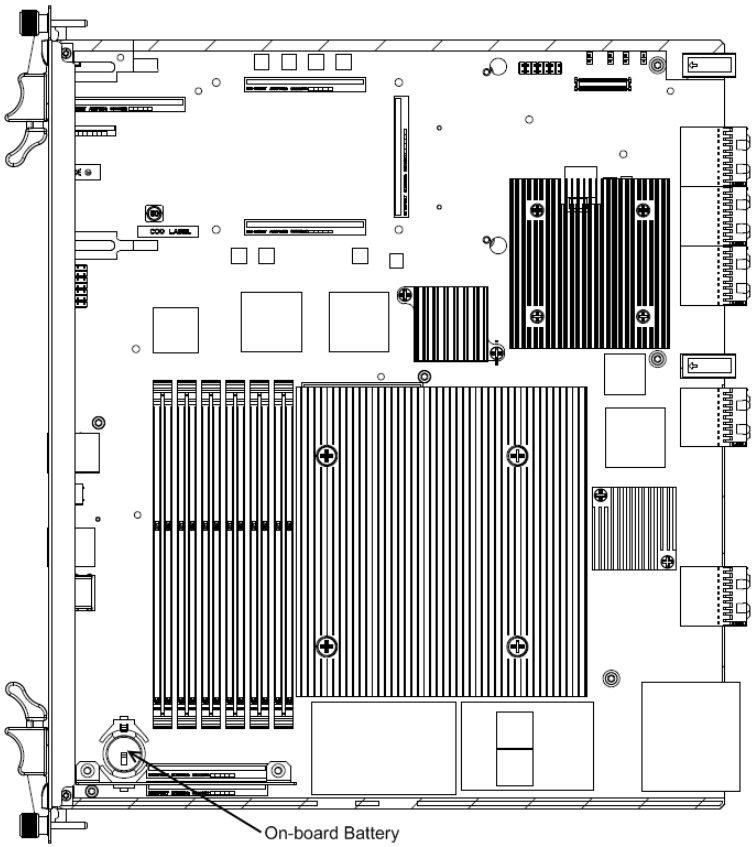
Filename	Description
atca-7367-amc-poped-ipmc.hpm	HPM file contains only the firmware image with AMC
atca-7367-amc-no-poped-ipmc.hpm	HPM file contains only the firmware image without AMC
atca-7367-c01-ipmc.hpm	HPM file contains only the firmware image for C01/C02
atca-7367-cpu-1.0.5.hpm	HPM file contains the version 1.0.5 BIOS image
atca-7367-fpga-12.bin	HPM file contains the version 12 FPGA image
Ipmitool-1.8.9-pps-8.tgz	PPS modified Ipmitool necessary for HPM upgrades on ATCA736X

A.1 Replacing the Battery

Some blade variants contain an on-board battery. Its location is shown in the following figure.

A battery-less variant based on SUPERCAP is available on demand.

Figure A-1 Location of On-board Battery



The battery provides data retention of seven years summing up all periods of actual data use. Artesyn Embedded Technologies therefore assumes that there is usually no need to replace the battery except, for example, in case of long-term spare part handling.

NOTICE

Board/System Damage
Incorrect replacement of lithium batteries can result in a hazardous explosion.
Therefore, replace the battery as described in this chapter.

Data Loss
If the battery does not provide enough power anymore, the RTC is initialized and the data in the NVRAM is lost.
Therefore, replace the battery before seven years of actual battery use have elapsed.

Data Loss
Replacing the battery always results in data loss of the devices which use the battery as power backup.
Therefore, back up affected data before Replacing the battery.

Data Loss
If installing another battery type other than what is mounted at board delivery may cause data loss. Other battery types may be specified for other environments or may have a shorter lifespan.
Therefore, only use the same type of lithium battery as is already installed.

Replacement Procedure

To replace the battery, proceed as follows:

1. Remove battery.

NOTICE

PCB and Battery Holder Damage
Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent this damage, do not use a screw driver to remove the battery from its holder.

2. Install the new battery following the "positive" and "negative" signs.

Related Documentation

B.1 Artesyn Embedded Technologies - Embedded Computing Documentation

The publications listed below are referenced in this manual. You can obtain electronic copies of Artesyn Embedded Technologies - Embedded Computing publications by contacting your local Artesyn sales office. For released products, you can also visit our Web site for the latest copies of our product documentation.

1. Go to www.artesyn.com/computing.
2. Under SUPPORT, click TECHNICAL DOCUMENTATION.
3. Under FILTER OPTIONS, click the Document types drop-down list box to select the type of document you are looking for.
4. In the Search text box, type the product name and click GO.

Table B-1 Artesyn Embedded Technologies - Embedded Computing Publications

Document Title	Publication Number
Basic Blade Services Software for the ATCA-7367 Programmer's Reference	6806800K42
ATCA-7367 Quick Start Guide	6806800K66
ATCA-7367 Safety Notes Summary	6806800K67
ATCA-7367 Release Notes	6806800K70

B.2 Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-2 Related Specifications

Organization	Document Title
PCI-SIG	PCI Local Bus Specification Revision 2.2 PCI-X Addendum to the PCI Local Bus Specification 1.0
PICMG	PICMG 3.0 Revision 2.0 Advanced TCA Base Specification PICMG 3.1 Revision 1.0 Specification Ethernet/Fiber Channel for AdvancedTCA Systems